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Analysis and Characterization of a SiGe BiCMOS Low Power Operational Amplifier

Archana Yarlagadda
University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Archana Yarlagadda entitled "Analysis and Characterization of a SiGe BiCMOS Low Power Operational Amplifier." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Syed Islam, Ethan Farquhar

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Thesis Presented for the
Master of Science Degree
The University of Tennessee, Knoxville

Archana Yarlagadda
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Abstract

Integrated circuit design for space applications can require radiation immunity, cryogenic operation and low power consumption. This thesis provides analysis and characterization of a SiGe BiCMOS low power operational amplifier (op amp) designed for lunar surface applications. The op amp has been fabricated on a commercially available 0.35-micron Silicon-Germanium (SiGe) BiCMOS process. The Heterojunction bipolar transistors (HBT) available in the SiGe process have been used in this op amp to take advantage of the total ionizing dose (TID) irradiation immunity and superb cryogenic operation, along with PMOS devices that show better TID immunity than their NMOS counterparts. The key features of the op amp include rail-to-rail output voltage swing, low input offset voltage, high open-loop gain and low supply current. The characterization of op amp is done for extreme temperatures and the results demonstrate that the op amp is fully functional across the lunar surface temperature range of −180°C to +120°C. The wide temperature operation of this op amp is tested using different bias current techniques such as proportional-to-absolute-temperature current, constant current and constant inversion coefficient current sources to investigate optimal biasing strategies for BiCMOS analog design. In addition, the SiGe BiCMOS low power op amp provides lower power consumption with the same or better unity-gain bandwidth when compared to a CMOS op amp with similar circuit topology.

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1 Chapter
INTRODUCTION

The need for electronics in environments that are outside the commercial or military specifications realm like space, deep-earth, deep-sea or volcanoes, for various research studies, has driven the design of extreme environment electronic systems. The constraints on these systems generally constitute their capability to work in such environments for a long time, with small size and low power consumption. This research work focuses on an operational amplifier for lunar applications that has wide temperature operation, radiation immunity and low power consumption. In general, an operational amplifier has a vast range of applications for signal processing in analog and digital circuits like in regulators, comparators, ADCs, DACs, etc.

1.1 Technology

The design of the operational amplifier has different choices of technology like CMOS, Bipolar, BiCMOS and others. Each technology has its advantages and disadvantages, and based on the requirement of the project, a particular technology is chosen. The advantages of CMOS over the bipolar design are high input impedance of MOSFETs, temperature adaptability, higher yield per die, package densities, and lower cost. The advantages of bipolar over CMOS design are higher transconductance, bandwidth, speed, noise performance, and better matching, thus lower offset voltage. The use of BiCMOS technology combines the advantages of CMOS and bipolar technology and provides high yield with an excellent trade-off between bandwidth and power consumption.

The use of homojunction Si BJT in the BiCMOS circuit will not meet the requirements of avionic application research, and an improved version of the BJT is required. The solution for this is the use of bandgap engineered heterojunction bipolar (HBT) devices in place of BJTs. Though there are many HBTs present in research, the Silicon-Germanium Hetero-junction Bipolar Transistor (SiGe HBT) is the first bandgap engineered device in Si technology used as an improvement over the Si BJT [1]-[2]. The SiGe HBT is obtained by implanting the Germanium material, which has a lower bandgap than Si, in the base region of the BJT. SiGe technology combines performance

improvement in the HBTs obtained from GaAs or InP, with the high yield, cost efficiency and improvement in processing obtained from conventional Si fabrication.

The improvements of the SiGe HBT can be attributed to the lowering of bandgap due to Ge, lower base resistance due to higher doping, and higher mobility of electrons and holes in SiGe than in bulk Si. The operational amplifier in this work was designed as a BiCMOS circuit in SiGe technology to make use of the excellent performance improvement offered by the HBTs for low power and extreme environment requirements.

1.2 Specifications for the Operational Amplifier

The requirement for the operational amplifier was to have high gain with low power consumption across a wide temperature range. For a precision operational amplifier, offset voltage and current were specified as constraints. The operational amplifier was designed to work inside a chip, to drive other stages, rather than an external load, and thus there was not a strict constraint on the output impedance. Table 1.1 gives a brief overview of the specifications for the work.

1.3 Flow of Thesis

Chapter 2: The constraints for the lunar environment and the devices used for the operational amplifier for these constraints is explained in Chapter 2. The comparison of the devices with their counterparts, with respect to working under the extreme environment, is also provided in Chapter 2.

Chapter 3: Design and analysis of the circuit, using the devices described, are in Chapter 3. Different stages in the operational amplifier like the input, output, frequency compensation and common-mode feedback are described in detail in this chapter.

Chapter 4: The characterization and simulation of the operational amplifier is presented in this chapter. Analysis of the factors affecting each parameter is presented along with simulation of these parameters across temperature.

Chapter 5: Experimental measurement of the fabricated chip for various parameters across temperature is presented in this Chapter. Description of the test set up used for these measurements and the comparison with simulation results is also provided. The effect of various current bias techniques on the circuit performance, in simulation and experiments, is also provided.

Table 1.1 Specifications for Operational amplifier

Parameter	Value	Units
Temperature range	−150 to +120	°C
Power consumption	< 1	mW
Supply current	< 1	mA
Open Loop Gain	> 60	dB
Bandwidth	> 2	MHz
Slew rate	> 2	V/μs
Input offset voltage	< 2	mV
Input bias current	< 200	nA
Power supply Rejection Ratio	> 60	dB

Chapter 6: Conclusion and Future work

2 Chapter
SiGe Devices for Extreme Environments and Low Power

Extreme temperatures (high or low), radiation environments (like in space), harsh chemical environments, high or low pressures, high vibrations, etc. can be considered as extreme environments. The circuit considered in this work is designed for the three most important conditions for space (specifically lunar surface) applications and they are low temperatures (up to −180 °C), high temperatures (up to +120 °C), and radiation (300 Krad total dose) [3]. Since it is for space applications it should have low power consumption for longer battery life. The purpose for this chapter is to describe how SiGe devices benefit the op amp in terms of its wide temperature range, power usage and radiation immunity. Comparison of the device parameters with their counterparts with respect to these conditions has been provided when appropriate.

The op amp under study is a SiGe BiCMOS operational amplifier with SiGe Heterojunction Bipolar Transistors (HBTs) and Si p−channel MOSFETs as the active devices. These devices are compared with the Si BJT and NMOS devices for desired specifications. Since the high temperature range of this work is same as that for a regular military specification, the in depth comparison and variations are focused toward cryogenic temperature operation.

2.1 Cryogenic Operation

2.1.1 Need for cryogenic circuits

It is important for space operations that the circuit works properly at cryogenic temperatures. The temperature ranges for different planets and moons are provided by NASA [4] and are shown in Table 2.1. The table shows that spacecraft exterior electronic devices (exposed to ambient) need to be able to work at cryogenic temperatures. The devices that are interior to the spacecraft will be maintained at −10 °C to +50 °C (in the warm electronics box (WEB)) and will not face such extreme temperatures under normal conditions [5].

Table 2.1 Planet/moon temperature data by NASA [4]

Planet/moon	Mean Temperatures
Earth's moon	+120 to −180 °C
Mercury (slow rotation)	−180 °C
Mars	−140 to +20 °C
Jupiter (cloud tops)	−140 °C
Europa (icy surface)	−188 to −143 °C
Saturn (cloud tops)	−185 °C
Titan	−180 °C
Uranus (cloud tops)	−212 °C
Neptune	−225 °C
Pluto	−236 °C

2.1.2 Effects on electronics

The lower temperature limit of the circuit is set by "carrier freeze-out" and "hot carrier" effects. Carrier freeze-out can occur due to the ionization temperature limit of the dopant element in the device [6]. If we take the device to lower temperatures the ionization of the dopants will decrease and there will be a temperature at which the ionization of the dopant will not happen. This means that there will be no carriers to carry the current and thus "carrier freeze-out" occurs. Increasing the doping concentration will help in pushing the freeze-out temperature to lower levels. Even before the lowest temperature for ionization of the carriers is reached, there are other effects that will come into play that change the performance of the circuit. Many parameters get affected due to temperature like the transconductance, mobility, bandwidth and others. Based on the devices and topology of the circuit, its response over temperature varies. The

devices are required to be chosen such that their response is in a desired quiescent operating region even at the extreme temperatures. In general, there is improvement in the parameters of semiconductor devices at lower temperatures. The benefits of HBT over BJT at these low temperatures are provided below.

2.1.2.1 HBT vs. BJT over temperature

The parameters of Si BJTs have variations like exponential decrease in current gain, increase in base resistance and decrease in frequency response with decrease in temperature. These effects, are detrimental for this design and, can be attributed to the carrier freeze-out in the base, bandgap narrowing in the emitter, and degradation of the minority carrier diffusivity in the base region at lower temperatures [7]-[9]. With these degradations, circuits designed for room temperature would not work as expected at lower temperature when designed with Si BJTs. With bandgap engineering in SiGe HBTs, as shown in Figure 2.1, these detrimental characteristics in BJTs are overcome in HBTs.

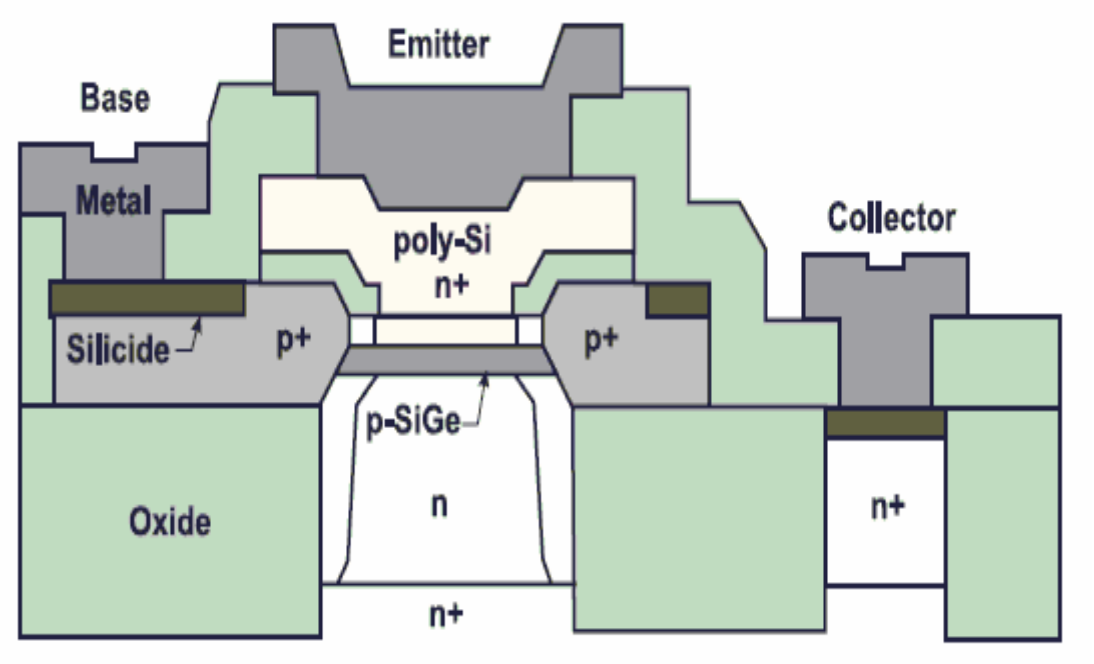


Figure 2.1 Schematic cross section of SiGe HBT (from [1])

The heavily doped base region offsets the bandgap-induced narrowing in the emitter and leads to an increase in current gain (β) with decrease in temperature in HBTs. The increase in β is also due to the Ge-induced band offset in the device [9].

$$\frac{\beta_{SiGe}}{\beta_{Si}} \cong \left\{ \frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,Ge(grade)} / kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \tag{2.1}$$

The increase in base resistance with decrease in temperature in case of Si BJTs is taken care of in HBTs by heavily doping both the emitter and base regions ($10^{19}/cm^3$).

The Ge grading across the base causes a built-in electric field which leads to the improvement of transit time of the carriers in base and thereby the frequency response improves at lower temperatures [9]. The reduction in the transit time is due to acceleration of carriers as shown in equation 2.2.

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\} \tag{2.2}$$

2.1.2.2 Temperature effects in MOSFETs

MOSFET devices can operate at cryogenic temperature, as the energy required for ionization of the carriers can be provided by the gate voltage rather than the temperature [10]. Thus, they can work below the freeze-out of the Si material. The concern in MOSFET devices is the hot carrier effect that occurs when carriers are accelerated beyond the normal velocity and the carriers enter the depletion region. High V_{DS} voltage leads to acceleration of carriers, which when they collide with atoms in silicon lattice results in depositing energy, and thus scattering of electrons and holes. When the energy is more than the dielectric potential across the gate, the carriers cross the barrier and get trapped in the oxide layer. This phenomenon will result hot-carrier induced degeneration such as change of transconductance. The mobility of carriers increases with decreasing temperature and the energy they attain at lower temperature is higher, making it easier for this phenomenon to occur. Note also that hot carrier effects are more pronounced in n-channel MOSFETs than in p-channel MOSFETs. The temperature at which the effects of hot carriers become significant, sets the lower temperature limit for the MOSFET devices. This value is below −180 °C and the MOSFET devices for this work are expected to work as desired. Even before the freeze-

out and hot carrier effects occur, there are other effects that occur at lower temperatures. The effects on parameters that are of prime concern for this work are described in this section.

MOSFET drain current can be estimated by [11]

$$I_{DS,sat} = \frac{\mu_n \varepsilon_{ox}}{2t_{ox}} \frac{W}{L} (V_{GS} - V_{THN})^2 \tag{2.3}$$

The parameters that change with temperature are the mobility and the threshold voltage. Both the threshold voltage and mobility increase with decrease in temperature. Since drain current is directly proportional to mobility and inversely proportional to threshold voltage, the V_{GS} value will decide which parameter will have higher impact on the drain current. For lower V_{GS} the threshold voltage change will dominate the drain current response and at higher V_{GS} the mobility variation does [11]. The actual lower limit of temperature for the particular application is set by the capability of the device to maintain the quiescent drain current value across the temperature range.

2.2 Low Power Consumption

Low power design is important not only for the space applications but in any portable system. Portable systems have to run on batteries, and the life of the battery is determined by the power consumption of the circuit/system that it is driving. Though there has been progress in the battery industry to improve battery energy density, this is not on par with the improvement in the device and circuit design for lower power consumption. The aim of this work is to design a low power operational amplifier and there are two approaches to attain this objective:

- System-level approach
- Device-level approach

The system level approach involving the use of a rail-to-rail class AB output stage for efficient use of power is presented in Chapter 3. The device level approach involves the use of HBTs in place of BJTs or NMOS devices to meet the specifications. The comparison of the devices is provided below.

2.2.1 HBT vs. BJT in terms of power consumption

High speeds (higher f_T) can be obtained in HBTs, when compared to BJTs, for the same collector currents. This implies that we can decrease the current required to

work at a given speed. Lower current requirement implies lower power consumption. The use of the Ge grading in the HBT leads to higher frequency of operation when compared to BJTs [1]. A good trade-off can be obtained between the high speed and power utilization in HBTs. Better β and f_T make the HBT more suitable for low power design. To improve the frequency response of the BJT, the base resistance R_b and the emitter capacitance C_e have to be reduced [12]. The transistor base region has to be widened and the doping increased to lower the resistance R_b, and the doping concentration has to be decreased in emitter region to decrease the capacitance C_e. The limitation of BJT is that these changes would decrease the current gain and also increase the transit time of carriers in base region, thereby providing negative results. These issues are overcome in HBT with wide-gap emitter or a narrow-gap base.

Under normal conditions, before any of the effects of extreme temperatures come into play, the current of the HBT (just as with a BJT) is provided by [6]

$$I_C = I_{CO} e^{\frac{qV_{be}}{nkT}} \tag{2.4}$$

where q is the electron charge, V_{be} is the base-emitter voltage, k is the boltzmann's constant, T is the absolute temperature and I_{CO} can be expressed as

$$I_{CO} = \frac{Aqn_i^2 D_n}{N_A W_B} \tag{2.5}$$

where N_A is the constant base doping, A is the area of the base-emitter, W_B is neutral base width, D_n is the electron diffusion co-efficient in the base and n_i is the intrinsic carrier concentration. In a hetero-junction device there is an improvement in the collector current over the homo-junction device and this can be represented as a ratio as shown below

$$\frac{I_{C,HBT}}{I_{C,BJT}} = \frac{N_{C,SiGe} N_{V,SiGe} D_{n,SiGe}}{N_{C,Si} N_{V,Si} D_{n,Si}} e^{\frac{\Delta E_V}{kT}} \tag{2.6}$$

where, N_C and N_V are the density of conduction and valence band states for respective materials. Thus we see an improvement in the collector current and thus the gain that can translate to lower power consumption when applied to circuit design.

2.2.2 HBT vs. NMOS in terms of power consumption

Consider the same circuit can be designed with NMOS devices in place of HBT devices. The low power of the BiCMOS op amp for a given bandwidth is because of the

high transconductance gain (g_m) of the HBT, especially in the first stage of an op amp. To obtain a comparable transconductance (at low current) from an NMOS, we would consider using the device in weak inversion saturation. The weak inversion saturation current required to get the g_m required can be calculated using equation 2.7 [13]

$$\frac{g_m}{I_d} = \frac{1}{nV_t} \tag{2.7}$$

where V_t = 26 mV is the thermal voltage and n = 1.4 (initial assumption). The g_m of the HBT obtained for a 10 μA current through the device is 360 μS. For an NMOS device, equation 2.7 shows that the current required is I_d = 13.1 μA for the same g_m.

The operating region and inversion level of the MOSFET can be identified using the inversion coefficient (IC) [14]. Based on the IC from the EKV model [13], the W/L required is 760. In the simulation to obtain a g_m of 360 μS, the current required by the input differential pair was 16 μA and thus the n = 1.6 (after calculation).

The simulated comparisons of the op amp parameters with both HBT and NMOS devices as the input are as shown in Table 2.2. The table shows that the SiGe HBT input device is clearly a better choice for the op amp design than the Si NMOS counterpart.

2.3 Radiation Effects in Devices

The basic effect of radiation (x-ray, gamma, or proton) is ionization of the material, which leads to formation of electron-hole combinations. The cumulative radiation, in an irradiated device, over a particular amount of time is called total ionizing dose (TID). The main effects of TID are creation of electron-hole pairs within the dielectric layers, formation of traps and net positive charge being trapped in the oxide.

Table 2.2 Comparison of HBT and NMOS input op amp ($g_{m,\,input}$ = 360 μS)

Parameters	HBT input	NMOS input
Power consumption	520 μW	800 μW
Phase Margin	51°	44°
Current through device	10 μA	16 μA

These effects can produce variations in device performance like threshold voltage shifts, leakage currents and noise. Instantaneous ionization caused by a single energy particle is referred to as single event effects (SEE). SEE will cause the sudden creation of electron-hole pairs in the path that the ion strike takes. When the energized particle passes through the active area of the device it can cause a transient pulse in the current. If this current is larger than the maximum value that the device can accommodate then the breakdown of the device may occur. The effects of irradiation on devices and their immunity are discussed in this section. Single event effects arise from the interaction of single particles (*e.g.* protons, neutrons or heavy ions) with the semiconductor causing either transient or permanent effects. The radiation sources for SEE testing include heavy ion, proton, and ion microbeam [17].

2.3.1 Radiation effects in BJT and HBT devices

The typical response of Si BJTs to ionizing radiation is degradation in the current gain characteristics of the transistor along with enhanced junction leakage current [16] and an increase in 1/f noise. Without any special hardening, HBTs show robustness to TID. HBTs exhibit a good response even after ionizing irradiations, without any additional radiation hardening processes, which can be attributed to the spatial arrangement of the layers in HBT rather than the presence of the Ge layer itself [15]. This good immunity to TID irradiation makes HBTs very attractive for space applications.

It has been shown in [16] that a SiGe HBT has much better radiation immunity than a Si BJT. For SiGe HBT, the experiments with fast neutron irradiations show I_C and β decrease, while I_B increases generally with an increasing neutron irradiation influence. For the Si BJT, I_B increases and β decreases much more than a SiGe HBT under the same fluence [16], and I_C increases at low V_{BE} bias and decreases at high V_{BE} bias. Enhanced ionizing radiation tolerance of the SiGe HBT, over conventional non-radiation hardened Si BJT, is attributed to the thin oxide/nitride spacer at the emitter-base and the high doping at the surface of the epitaxial base region of the device [17], refer to Figure 2.1.

The SiGe HBT devices show SEE sensitivity due to their vertical cross-sectional volume [18]. It requires special radiation hardening processes for SEE radiation immunity.

2.3.2 Radiation effects in MOSFET devices

When MOSFETs are exposed to TID irradiation, the gate oxide layer will be ionized. Electrons being more mobile than holes can drift out of oxide and disappear, but a small portion of holes will get trapped in the oxide. These trapped positive charges over a period of time accumulate and, in case of the NMOS device, will increase the net positive charge applied to the gate. If enough charge accumulates, the NMOS device will remain “ON” undesirably even when the applied voltage is low. For PMOS devices, the charge accumulated and associated field will have to be higher than the applied gate voltage to turn “OFF” the device. Hence, there is more head room for designing with PMOS devices and they show more TID immunity than NMOS devices [19]. The effect of the irradiation on the gate oxide layer was significant when the thickness of gate oxide and the channel length were large. However, with the constant scaling down of CMOS devices, the thickness of the gate oxide is so thin that the trapped oxide effect in gate oxide has become very low in modern CMOS processes.

In more recent devices, the radiation-induced oxide trap charge in the shallow trench isolation (STI) oxide of the PMOS and NMOS devices has become significant. The STI oxide that encloses the PMOS and NMOS devices is much larger than the gate oxide thickness. STI trapped charge can cause a parasitic MOSFET in parallel with the actual device. This parasitic device will induce a leakage current. For this oxide trapped charge is higher at lower temperature, it can limit the lower temperature of the circuit.

PMOS and NMOS devices show similar effects to SEE. Sudden high energy particle bombardment can occur in any direction and when it occurs in the active region, it will cause a sudden current due to electron-hole combinations and can cause oscillations in the circuit or permanent damage to the device.

The effects of radiations and cryogenic temperatures on devices, and the low power consumption of HBTs for the BiCMOS circuit is discussed in this chapter. The next chapter explains each stage in the BiCMOS op amp, designed using the devices explained in this chapter.

3 Chapter

Design and Analysis of SiGe BiCMOS Low Power Op Amp

The BiCMOS low power operational amplifier has been implemented in the SiGe 0.35-μm process. Its circuit topology is inspired from [20] and has been modified and redesigned to meet the required specifications. It makes use of various features of HBTs and PMOS devices such as TID immunity, high gain, extreme temperature performance capability, and others that have been dealt in depth in Chapter 2. In this chapter the design of the circuit using these devices is described.

3.1 Stages of Operational Amplifier

The SiGe BiCMOS low power operational amplifier was designed as a two-stage op amp (number of effective gain stages are two), with input and output stages providing the required open-loop gain. The other stages present are a common mode feedback circuit (CMFB), an RC tracking compensation, and a biasing circuit for these stages. These stages are designed for stability and performance requirements. A block diagram of the op amp is provided in Figure 3.1 and the analysis of each stage is given in the sections that follow.

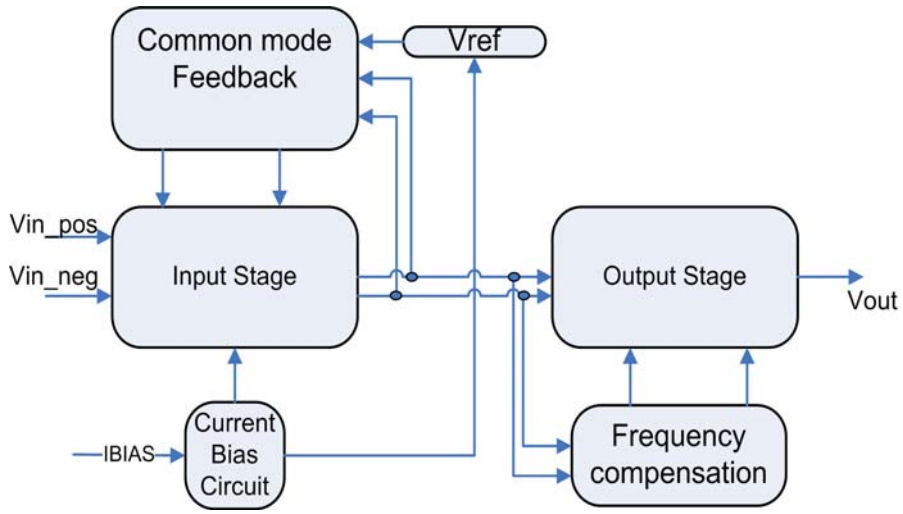


Figure 3.1 Block diagram of Op amp

3.1.1 Input stage

The input stage is a fully differential gain stage as shown in Figure 3.2. It provides high gain and wide input common-mode range. The design of the input stage and the devices chosen determine performance parameters such as voltage and current offset, noise, CMRR, ICMR, open-loop gain and input impedance.

Device selection discussion was presented in Chapter 2 for the op amp design in terms of operating region. Device sizing is being discussed in this section. The next chapter deals with how the design affects the characteristic parameters.

The input stage in this op amp is designed to provide a major share of the open-loop gain, as there are only two gain stages. The gain of the second stage is dependent on the output load and thus it becomes important that the voltage gain of the input stage be well controlled and large.

The gain of the input stage is explained with reference to Figure 3.2 and can be given as:

$$A_{v1} = \frac{R_{leq}}{(r_{e:Q1} + r_{e:Q2})} \tag{3.1}$$

$$R_{leq} = r_{ds:M1} \,||\, r_{o:Q1} \tag{3.2}$$

With input bias current I_{TAIL} =20 μA, the parameters were calculated as $r_{e:Q1} = r_{e:Q2}$ = 5.2 KΩ, $r_{ds:M1}$ = 4.5 MΩ, $r_{o:Q1}$ = 12 MΩ and thus the effective gain of the first stage is 320 V/V or 50 dB at room temperature.

The HBTs and the PMOS devices are designed such that, when the common-mode input voltage is within the op amp's ICMR range, they are in the forward-active and saturation regions, respectively. This is true for the devices in the op amp, with the exception of the MOSFETs in the compensation network which are in the triode region to form active resistors. The Q1-Q2 and M1-M2 devices are well matched pairs. The effect of this design on the input parameters is explained in Chapter 4.

3.1.2 Common-mode feedback circuit

The common-mode feedback (CMFB) is an essential portion of the op amp that ensures that the output nodes of the input differential pair, N1 and N2, are not floating and that they remain at a well-controlled quiescent voltage value. The operation of the common-mode feedback can be explained with the help of Figure 3.3. A qualitative

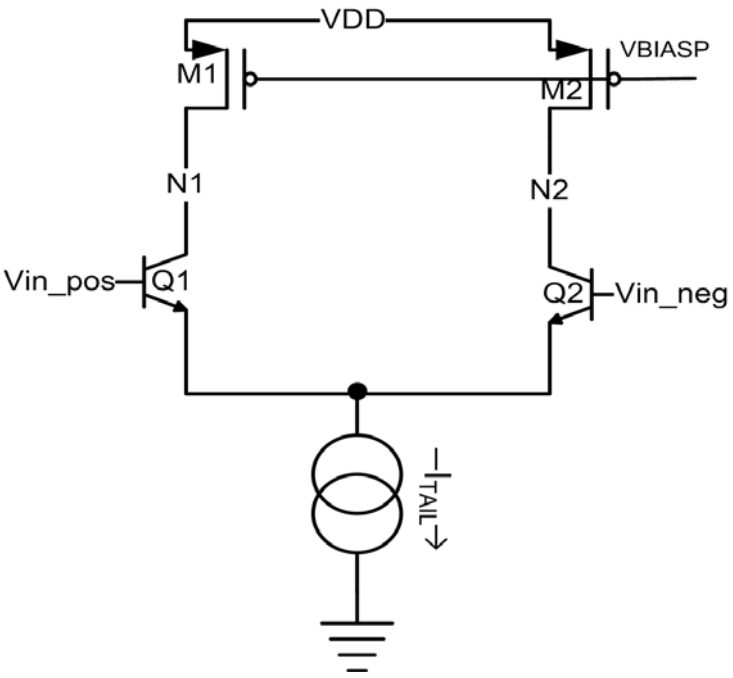


Figure 3.2 Input stage of op amp

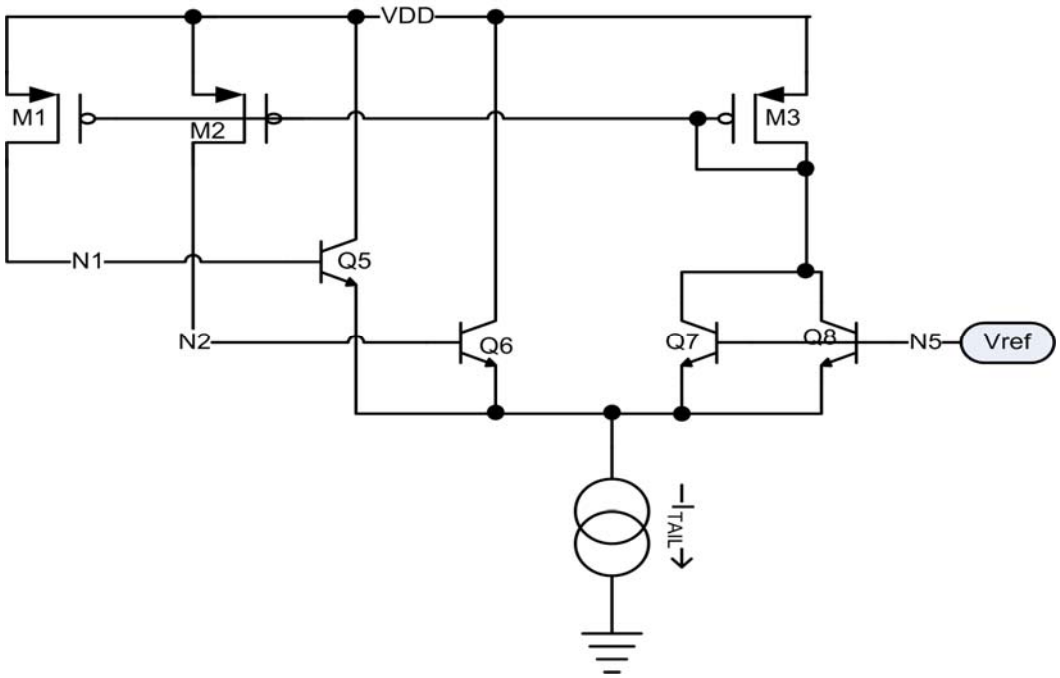


Figure 3.3 Common mode feedback circuit of op amp

description of how the CMFB of the circuit helps maintain the voltages at different nodes within the input stage is provided below.

If the common-mode voltage for nodes N1 and N2 were to drift toward V_{DD}, this would result in increased current in Q5 and Q6. Since the bias current remains constant, the current in Q7 and Q8 will decrease, and subsequently V_{SG} of M3 will decrease. Thus the gate potential V_G of M3, M1 and M2 would move toward V_{DD}. The inverting gain action of common-source (CS) amplifiers M1 and M2, however, will then cause nodes N1 and N2 to move away from V_{DD}, thus counteracting their original common-mode drift toward V_{DD}, therefore demonstrating the negative feedback action of the CMFB circuit. A similar sequence takes place when there is a downward variation in the common-mode voltage at nodes N1 and N2. The CMFB thus regulates the common-mode voltage of N1 and N2.

3.1.3 Output stage

The output stage is designed such that it consumes low quiescent power during standby and has good driving capability along with high gain. The rail-to-rail output voltage range and Class-AB biasing ensure efficient use of the supply voltage. The current in the output stage is dependent on the input bias current and is independent of the supply voltage. The method in which this is achieved is explained with the help of the Figure 3.4.

The common-mode feedback circuit described above maintains the voltages at nodes N5, N1, and N2 at the same potential. Since the sources of the three devices M4, M8 and M10 are at the same potential (V_{DD}) and their gates are maintained at same potential by the CMFB, we have

$$V_{GS:M4} = V_{GS:M8} = V_{GS:M10} \tag{3.3}$$

This implies that,

$$I_{D:M4}\left(\frac{L}{W}\right)_{M4} = I_{D:M8}\left(\frac{L}{W}\right)_{M8} = I_{D:M10}\left(\frac{L}{W}\right)_{M10} \tag{3.4}$$

Thus, we can make the current output branch independent of the supply by making the current in device M4 independent of supply voltage. The current in the Vref branch is set by the Q10 device, which mirrors a fraction of the input bias current. In this circuit,

$$\left(\frac{W}{L}\right)_{M10} = 12\left(\frac{W}{L}\right)_{M4} \tag{3.5}$$

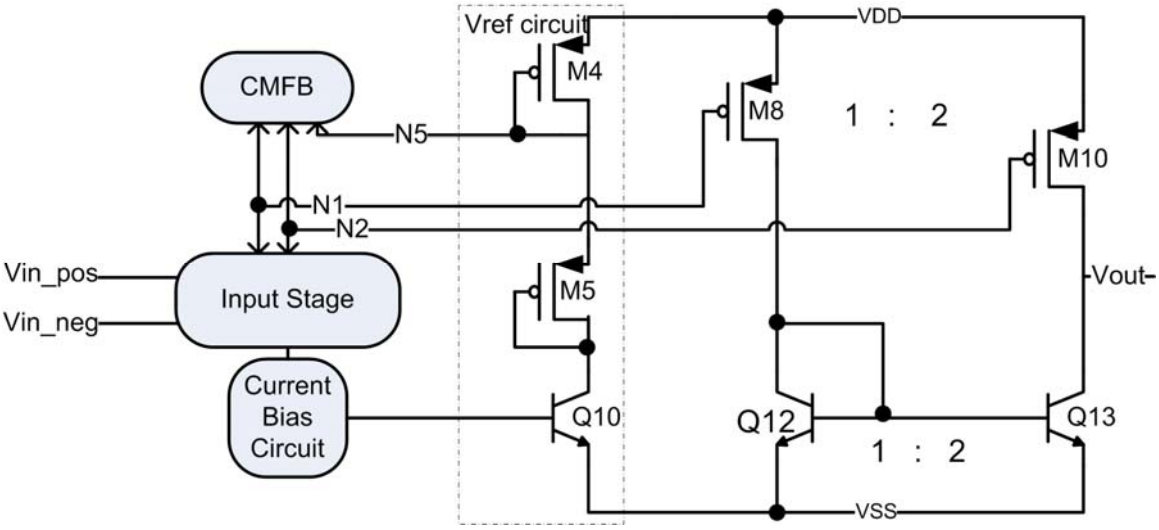


Figure 3.4 Simplified output stage of op amp

And the device size of Q10 is such that it mirrors 1/4th of the input bias current. Thus the current in the output rail is 3 times the current bias current provided into the op amp. The op amp was characterized with an input bias current of 20 μA and the output current was observed to be 60 μA, as expected. This provides the required drive for the op amp.

The gain of the output stage can be obtained as follows by referring to Figure 3.4. If we consider the gain path through M8 we see that the gain is

$$Avout = \frac{g_{m:M8} \times 2}{g_{0:M10} + g_{0:Q13}} \tag{3.6}$$

If we consider the gain path through the PMOS M10 we find that the gain is

$$Avout = \frac{g_{m:M10}}{g_{o:M10} + g_{o:Q10}} \tag{3.7}$$

Considering that

$$\left(\frac{W}{L}\right)_{M10} = 2\left(\frac{W}{L}\right)_{M8} \tag{3.8}$$

We find that the over-all gain through the output stage is effectively the same through both the paths as is shown in the equation above.

For the device dimensions and biasing utilized in this design, the estimated values obtained for the above mentioned parameters were as follows: $g_{m:M10} = 500\mu S$, $g_{m:M8} = 250\mu S$, $g_{o:Q13} = 550nS$, and $g_{ds:M10} = 950nS$.

Using these values the gain of the output stage (no load) was about 330 V/V or 50 dB.

The output stage also determines the output impedance of op amp and by looking at the output stage we see that

$$R_{out} = \frac{1}{g_{o:M10} + g_{o:Q13}} \tag{3.9}$$

Output impedance was calculated to be 600 KΩ and thus cannot drive very heavy output loads. On-chip output loads are usually capacitive, otherwise we will have to use an buffer stage to drive low impedance loads.

3.1.4 Frequency compensation

The requirement of the op amp is to have unity-gain stability, i.e. stability when the output is fed back directly to the input without attention. Considering the circuit stages explained so far without any frequency compensation, the estimated phase margin (PM) from the open-loop Bode response was 2°. For such a low phase margin the op amp would not be stable in the unity-gain configuration. The dominant nodes in the circuit and the method of compensation are explained with the help of Figure 3.5.

The dominant nodes in the circuit are the output nodes of the input differential pair (N1, N2) and the output node (N10). The pole at nodes N1 and N2 can be given as:

$$f_{N1,N2} = \left(\frac{1}{2\pi R_{1,2} C_{1,2}} \right) \tag{3.10}$$

where

$$R_1 = r_{0:M1,M2} \,||\, r_{0:Q1,Q2} \tag{3.11}$$

$$C_1 = C_{ce:Q1,Q2} + C_{gd:M10,M8}(g_{m:M10,M8}(r_{0:M10,M8} \,||\, r_{o:Q13,Q12})) \ . \tag{3.12}$$

The pole at the output of the output stage can be given as

$$f_{N10} = \left(\frac{1}{2\pi R_{10} C_{10}} \right) \tag{3.13}$$

where

$$R_{10} = r_{o:M10} \,||\, r_{o:Q13} \tag{3.14}$$

$$C_{10} = C_{gd:M10} + C_{ds:M10} + C_{ce:Q13} + C_L \tag{3.15}$$

To increase the phase margin, $f_{N1,N2}$ must be reduced (to lower frequency) and f_{N10} must be pushed higher in frequency, preferably beyond the crossover frequency. This

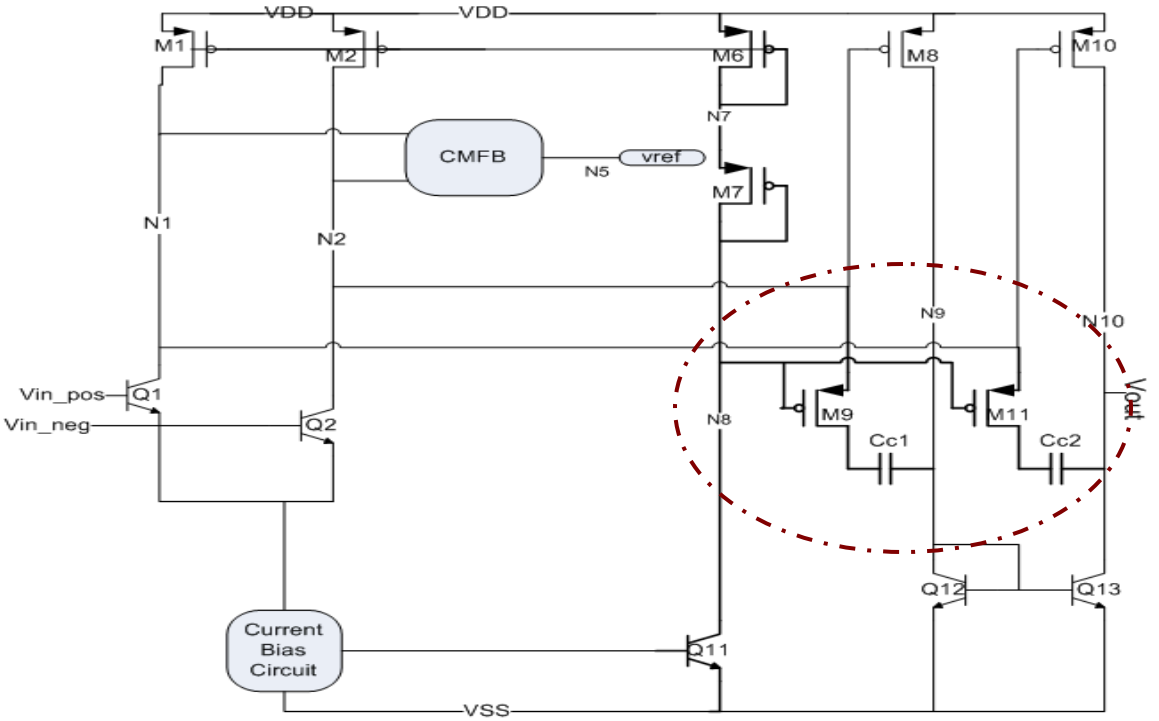


Figure 3.5 Frequency compensation circuit of the Op amp

can be obtained by using a Miller compensation capacitor C_c and choosing its value to implement pole splitting as required for the PM improvement.

The compensation capacitor adds a zero in the right half-plane (RHP), thus effecting the stability and settling time of the circuit. To avoid adverse effects on settling time, the RHP zero has to be nullified or transformed to a left half-plane (LHP) zero. The zero frequency is

$$f_z = \left(\frac{1}{2\pi C_c \left(\frac{1}{g_{m:M10}} \right)} \right) \tag{3.16}$$

and by adding a resistor R_z, the frequency of the zero becomes

$$f_z = \left(\frac{1}{2\pi C_c \left(\frac{1}{g_{m:M10}} - R_z \right)} \right) \tag{3.17}$$

Thus, if $R_z = \frac{1}{g_{m:M10}}$, the zero is pushed to an infinite frequency (nullified). The problem that arises due to the use of a resistor is maintaining the value across variations in process, temperature, and voltage. For this reason, the resistor is implemented with a MOSFET operating in triode region that effectively has a resistance of $\frac{1}{g_m}$. The W/L of the device is chosen such that $\frac{1}{g_{m:z}} = \frac{1}{g_{m:M10}}$. In the circuit shown in Figure 3.5, C_{c1} and C_{c2} are the compensation capacitors and M9 and M11 are the active resistors for zero cancellation.

The effective dominant pole, after the addition of capacitors C_{c1} and C_{c2} at the output nodes of the input differential pair, is given in equation 3.18 [20]

$$f_{dom} = \left(\frac{1}{2\pi R_{out1}(C_{M1} + C_{M2})} \right) \tag{3.18}$$

where R_{out1} is the output impedance of the input differential stage and C_{M1} and C_{M2} are the effective Miller capacitances. The capacitors are given as $C_{M1} = (1 + g_{m:M8} g_{m:M9})(C_{c1}/2)$, which is one-half of the Miller capacitance due to C_{c1}, and $C_{M2} = g_{m:M10} R_L C_{c2}$, which is the effective Miller capacitance due to C_{c2}. The entire schematic of the op amp is shown in Figure 3.6. The resistors shown at the emitters of the current mirroring HBTs in the current bias circuitry are for better matching of the current mirrors.

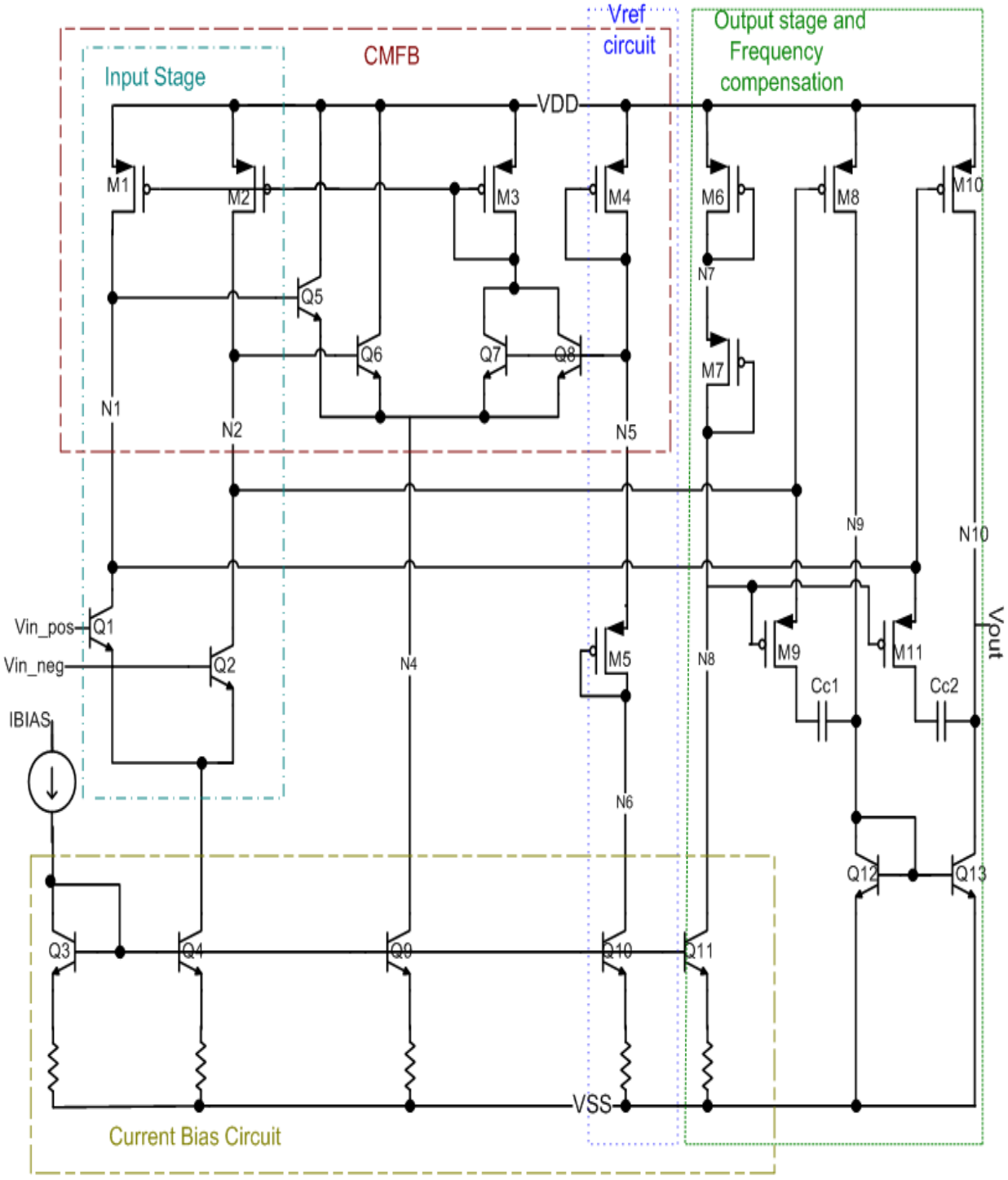


Figure 3.6 Complete schematic of the op amp

4 Chapter
Characterization and Simulation

The non-ideal characteristics of an operational amplifier and the factors affecting these parameters are provided in this chapter, specifically with respect to the SiGe BiCMOS low power op amp. A brief comparison of a CMOS counterpart of this BiCMOS op amp under study is provided as well. A non-ideal operational amplifier with DC offsets and noise parameters can be represented as in Figure 4.1 [21]. The parameters mentioned in this figure, along with other parameters like slew-rate and input common mode range, are discussed.

4.1 Slew Rate (SR)

Slew rate is defined as the rate of change of the output voltage. It is a result of limited current flowing across a particular capacitor. Considering the circuit in Figure 3.6, it can be seen that the limiting currents are the currents in compensation capacitors and the current flowing through the load capacitor. The actual slew rate is determined by whichever current, capacitor combination is responsible for slowest variation in the output voltage. In general, for any capacitor

$$\frac{dV_{capacitor}}{dt} = \frac{I_{\max}}{C} \tag{4.1}$$

Considering a negative-going voltage swing of the input Vin_pos, and the corresponding negative-going voltage swing at the output, the slew rate for high-to-low transistions of the output would be limited by the currents flowing across the capacitors C_{C2} and C_L as given in equation 4.2.

$$SR = \min\left(\frac{I_{e:Q4}}{C_{C2}}, \frac{-I_{e:Q4} + I_{e:Q13}}{C_L}\right) \tag{4.2}$$

Similarly for a positive-going swing at the non-inverting input Vin_pos and associated positive-going swing at the output, the slew rate would be,

$$SR^{+} = \min\left(\frac{I_{e:Q4}}{C_{C2}}, \frac{I_{d:M10} - I_{e:Q4} - I_{e:Q13}}{C_L}\right) \tag{4.3}$$

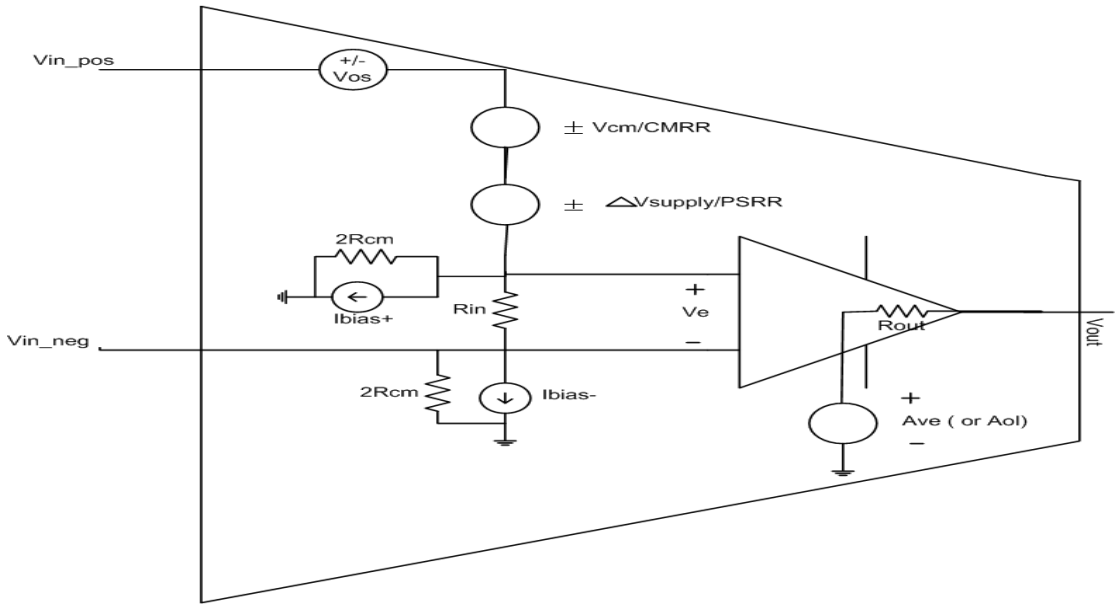


Figure 4.1 Non Ideal parameters of Operational amplifier [21]

The tail current $I_{e:Q4}$ is lower than the output branch current $I_{4:Q13}$($I_{d:M10}$), which means that the slew rate is determined mainly by the tail current of the input differential pair and the compensation capacitor C_{C2}. Thus, when C_L is not too large, we have an effective slew rate of

$$SR = \left(\frac{I_{e:Q4}}{C_{C2}} \right) \tag{4.4}$$

With an input tail current bias of 20 μA, the simulated slew rate of the positive-going edge was obtained as 5.5 V/μs and the negative-going edge as 3 V/μs. The simulated slew rate is provided in Figure 4.2 along with the change of slew rate across temperature.

The slew rate is related to the transconductance and unity-gain crossover frequency as given by equation 4.5.

$$SR = \frac{I_{Q4}}{g_{m:Q1}} \omega_c \tag{4.5}$$

where, I_{Q4} is the tail current of the input differential pair, $g_{m:Q1}$ is the transconductance of transistor Q1, and ω_c is the unity-gain crossover frequency. The equation predicts that the SR is lower in the case of an HBT input operational amplifier as compared to its

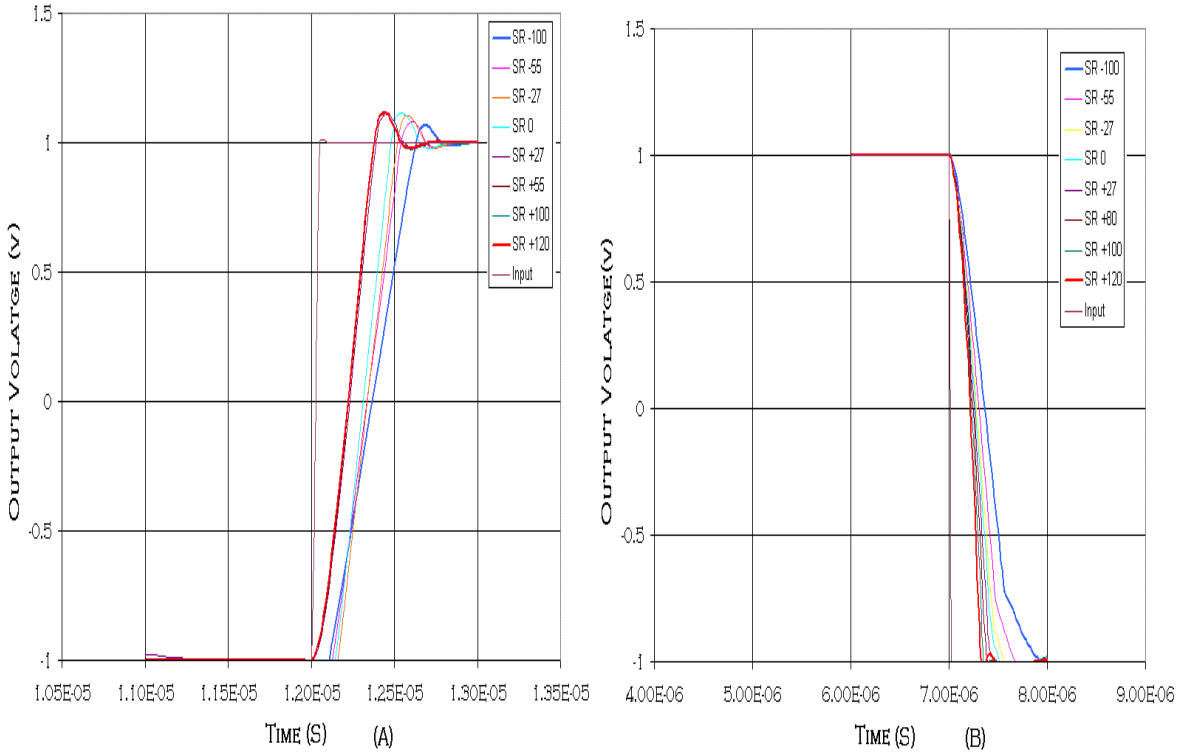


Figure 4.2 Slew Rate positive (A) and negative(B) edge variation across temperature

CMOS counterpart, and this was observed in simulations. The positive-going slew rate of the BiCMOS op amp is 5.5 V/μsec and the SR+ of the CMOS counterpart op amp of is 7 V/μs [22]. Equation 4.5 also implies that the slew rate may increase with temperature (consider transconductance variation over temperature). This is observed in the simulated results shown in Figure 4.2. The SR at 120° C is the highest and the SR at −100° is the lowest in Figure 4.2.

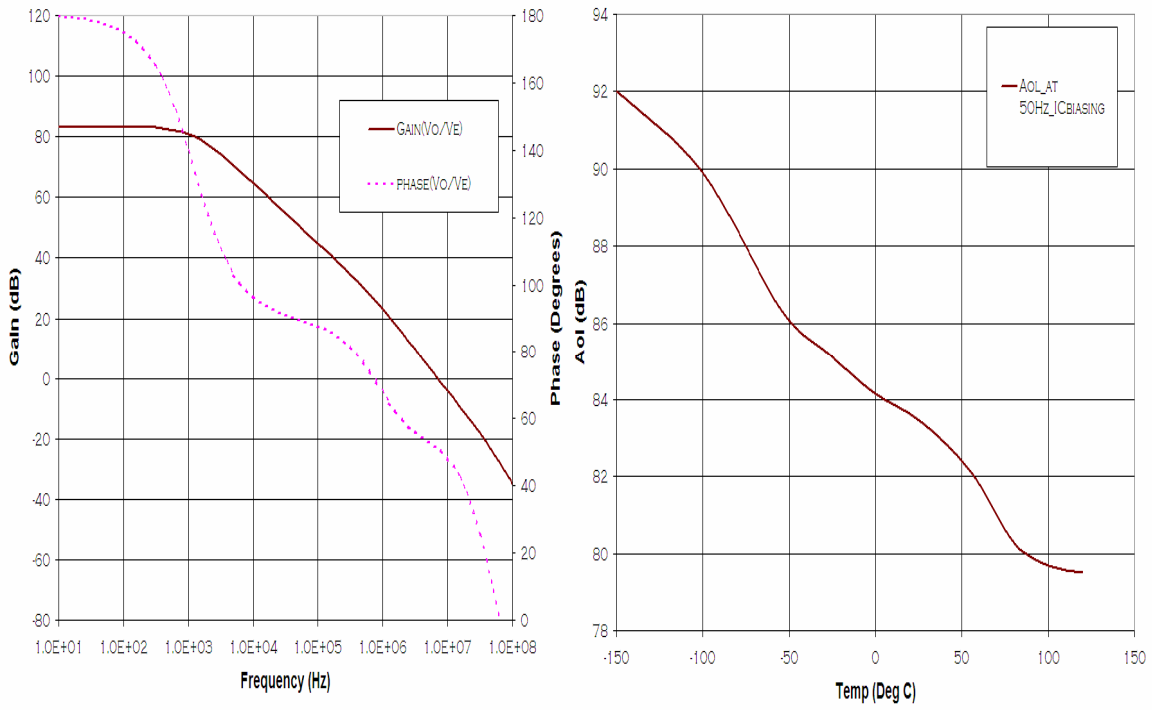
4.2 Open-loop Gain (Aol) and Phase Margin (PM)

The gain of an ideal op amp is infinite, but this is not the case in a practical op amp. The gain of the op amp is represented by A_{ve} (same as A_{ol}) as shown in the Figure 4.1. The gains of the input and output stages were discussed under their respective sections in Chapter 3. The overall gain can be expressed as

$$A_{ol} = A_{v1} \times A_{Vout} \tag{4.5}$$

where A_{v1} = input stage gain as given in equation 3.1 and A_{Vout} = output stage gain as given in equation 3.7. The open-loop gain was 84 dB at room temperature for an bias input current of 20 μA and the graph of the open-loop gain is shown in Figure 4.3(A).

The op amp's poles and zeros were discussed in section 3.5 and the overall frequency response for the op amp was obtained as shown in Figure 4.3(A) and the change of the gain across temperature at 50 Hz is shown in Figure 4.3(B). From the simulated graphs it was observed that the phase margin is around 52° and the unity-gain crossover frequency is 7 MHz. The gain increases with decrease in temperature since the transconductance of the HBT devices increases with the decrease in temperature. Since r_e is inversely proportional to transconductance, r_{e1} and r_{e2} decrease with lowering temperature. From equation 3.1 we see that this situation will improve the gain of the input stage and thus the overall open-loop gain.



(A) (B)

Figure 4.3 (A) Op amp simulated frequency response (B) and the open-loop gain at 50 Hz across temperature

4.3 Input offset voltage (V_{OS})

When the input is zero, an ideal op amp's output would be zero. However, for an non-ideal op amp, the output has a particular value of voltage even when the input is zero. This voltage is referred back to input and is represented as a voltage source in series with the non-inverting input side of op amp as shown in Figure 4.1. This is the offset voltage V_{OS} and is composed of two types of offsets: systematic and random offset [23]. The former exists in the circuit due to the design, irrespective of the matching in the devices, and the latter results primarily from the mismatch in the balanced paths of the differential pair.

In general, the systematic offset of a bipolar input op amp is lower than its MOSFET counterpart due to the higher gain from each stage [23]. For this work, systematic offset is a result of imbalance or asymmetry in the op amp circuit topology resulting from the differential to single-ended signal conversion in the output stage. This offset will be small if the gain of the input stage is high. Such is the case for this design thanks to the HBT input stage. Simulations show the systematic offset as 12 μV for the HBT input op amp, significantly lower than the 30 μV for its MOSFET input CMOS op amp counterpart [22]. The systematic offset for the amplifier is shown in Figure 4.4. The sudden change in V_{OS} at the −55°C is due to a change in the model files used for simulation at lower temperatures. A linear trend line has been included in the Figure 4.4 to show the trend of V_{OS} variation across temperature.

The random offset results primarily due to mismatch between the two paths of the differential input stage, particularly device mismatch. For the same order of percentage variation in the currents, the offset voltage that results in the bipolar transistor pairs are half an order of magnitude lower than MOSFET transistor pairs [24]. Considering Δ as the percentage mismatch, the offset voltage can be described by equation 4.6 [23],

$$V_{OS} = \frac{I}{g_m}\Delta \tag{4.6}$$

where the current to transconductance ratio I/g_m, is equal to kT/q (26 mV at room temperature) for the BJT and $(V_{GS}-V_T)/2$ (a bias dependent quantity that is normally 100 to 500 mV) for the MOSFET. Thus the random offset voltage is also lower for a BJT differential input pair than its MOSFET counterpart.

Monte-Carlo simulations were performed to measure the offset across process and matching variations. The values were obtained for −55°C to 120°C for 100 iterations and these values were averaged for all the iterations and the histogram of the results is provided in Figure 4.5. It was observed that the random offset accounts for most of the total offset of the op amp and the average value is 600 μV for the SiGe BiCMOS low power op amp. A similar set of simulations on the MOSFET counterpart op amp predicts its V_{OS} as 1.3 mV [22]. These results show that the input offset voltage is lower for the BJT (or HBT) input differential pair op amp than a comparable MOSFET input op amp.

4.4 Input Bias and Offset Currents

One benefit of a bipolar input op amp is the relatively low offset voltage. However, one must deal with the input bias current and input offset current that is negligible in the MOSFET input pair op amp. Input bias current may result in large voltage offset when they flow through large resistors and hence become an important parameter for characterization for BJT input operational amplifiers.

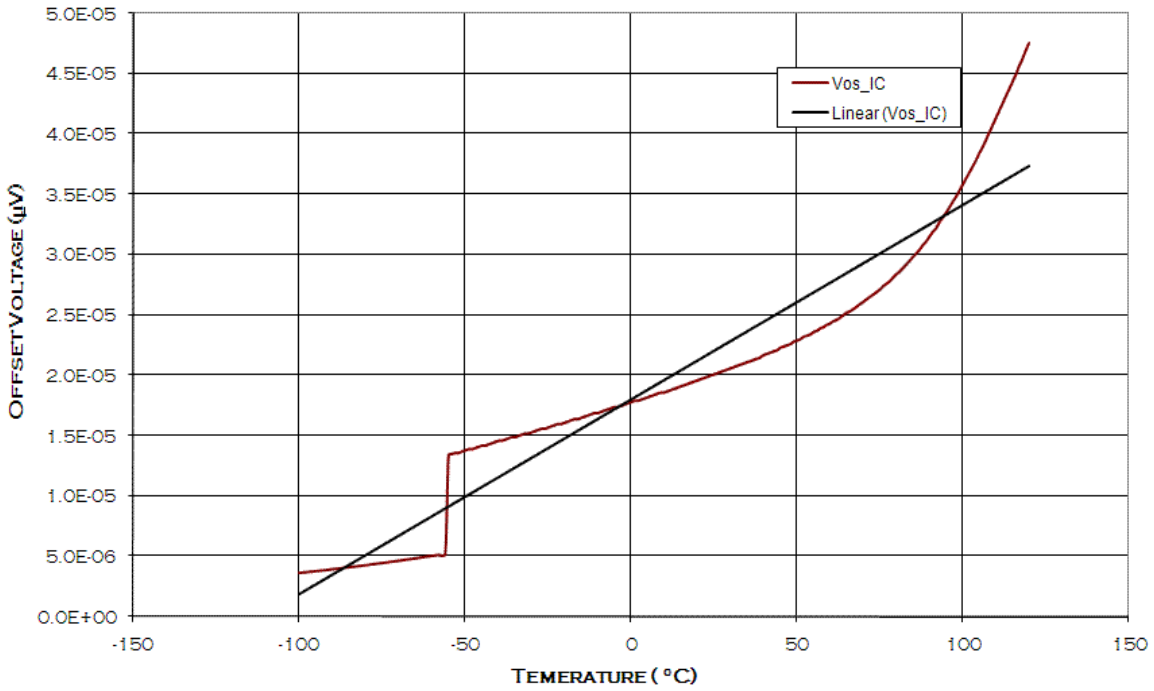


Figure 4.4 Simulated systematic input offset voltage

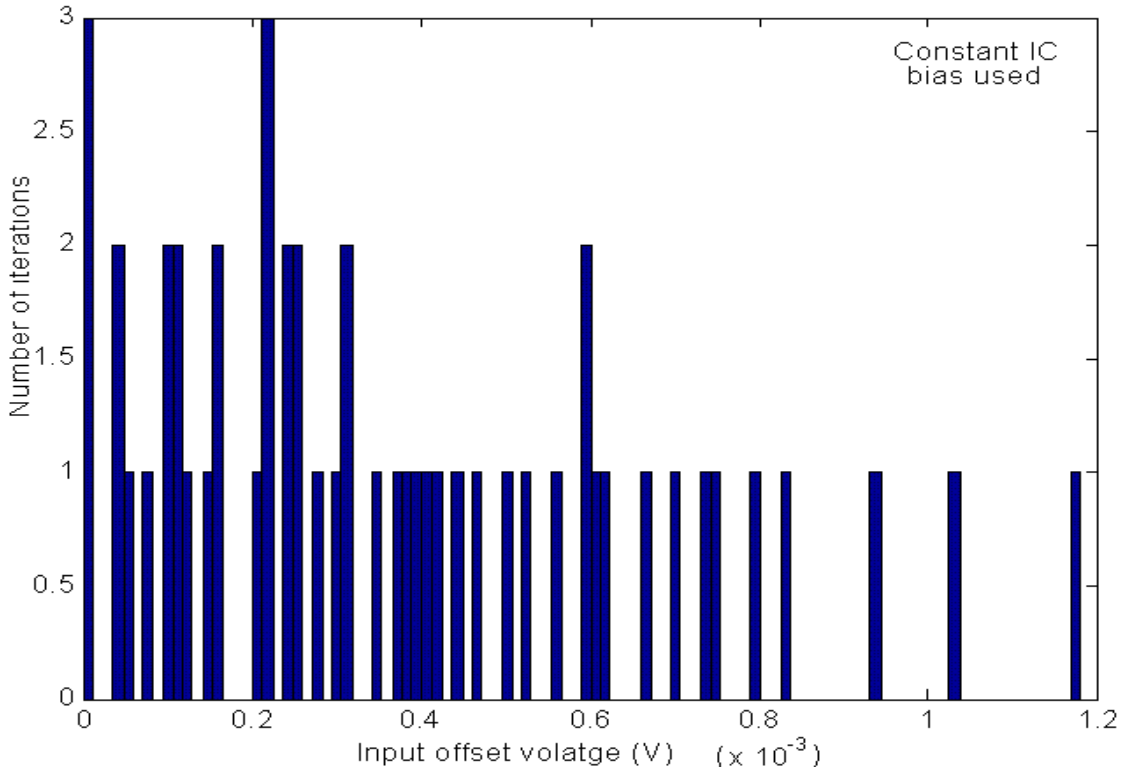


Figure 4.5 Histogram of Monte-Carlo simulation (process and matching) for V_{os}

In the SiGe BiCMOS op amp under study the input bias current is the base current of the transistors Q1 and Q2, referring to Figure 3.6. All the HBTs used in this design are of the same size with an emitter area of 2.5 μm X 0.5 μm. The beta value for these transistors was nominally 100 for forward active operation. The characterization of the bias current was done with a Q1/Q2 collector current of 10 μA. This provides the expected input bias currents in the positive and negative terminals of the op amp as 100 nA. In simulation these currents were about 91 nA at 27 °C, flowing into the positive and the negative terminals as shown in Figure 4.6. The positive and negative bias currents are overlapping in Figure 4.6.

The input currents flowing into both inputs are ideally equal. Due to mismatch there is a small difference between the two input bias currents and this difference is known as the input offset current. This offset current in simulation was nominally 55 pA.

4.5 Power Supply Rejection Ratio (PSRR)

In practice, noise is likely introduced on to the supply voltage rails. These changes in voltage of power rails can feed through to the output of the op amp [11]. High-

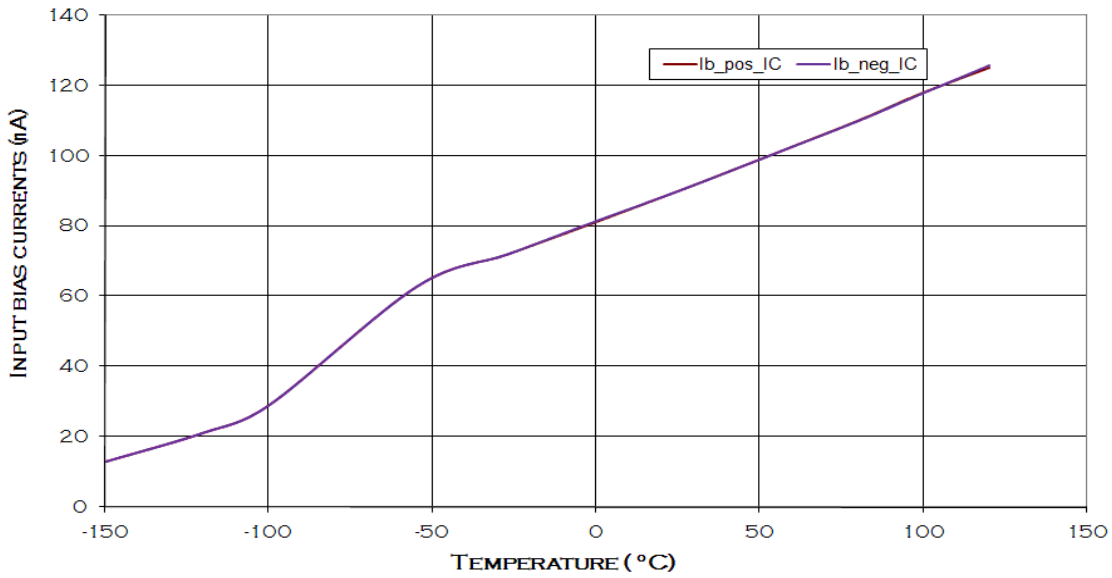


Figure 4.6 Simulated positive and negative input bias currents

frequency supply noise can couple through the compensation networks to the output of the op amp. The op amp's ability to reject power supply noise is generally quantified by power supply rejection ratio (PSRR). PSRR+ and PSRR- are defined by equation 4.7. These parameters were simulated and their variation across frequency is presented in Figure 4.7.

$$PSRR^{+} = \frac{A_{ol}}{\left(\frac{V_{OUT}}{V_{DD}}\right)}, PSRR^{-} = \frac{A_{ol}}{\left(\frac{V_{OUT}}{V_{SS}}\right)} \tag{4.7}$$

4.6 Input and Output Resistances

4.6.1 Input resistance

The input resistance of an ideal op amp is infinite but in practice is finite, though typically high in value. The open-loop input resistance for the op amp under study (see Figure 3.6) is the resistance looking into the bases of Q1 and Q2 at the positive and negative input terminals, respectively, with the other terminal grounded. The input resistance looking into the base of Q1 while the base of Q2 is grounded is described by

$$R_{in,OL} = r_{b:Q1} + (1+\beta_{Q1})(r_{e:Q1} + r_{e:Q2}) \tag{4.8}$$

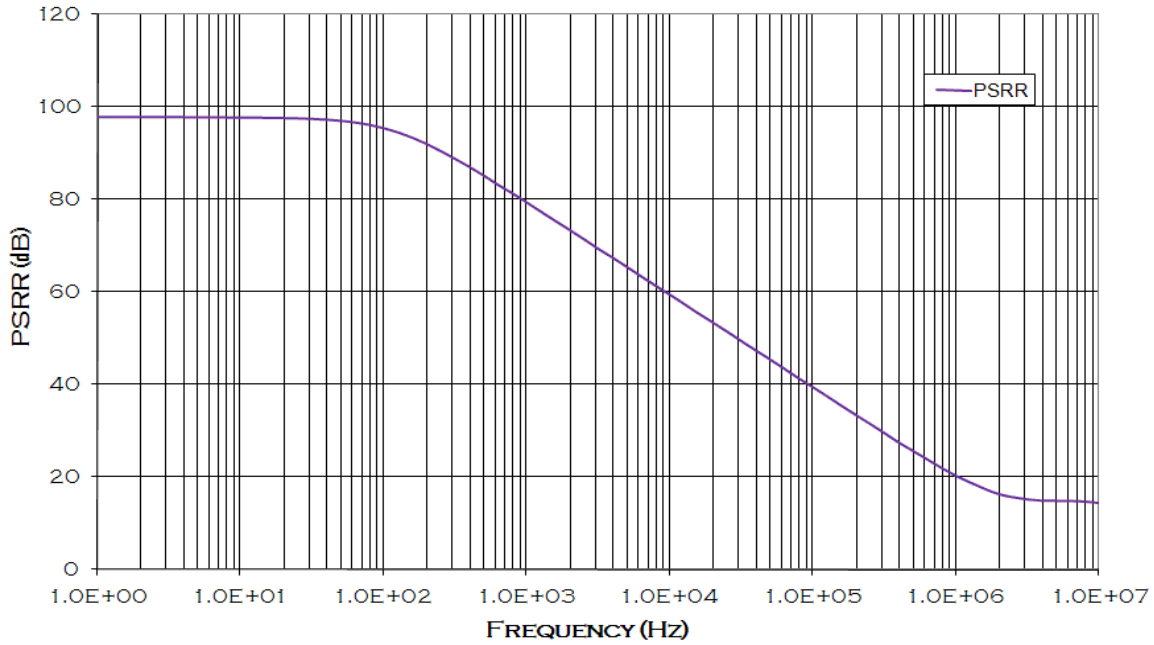


Figure 4.7 PSRR vs Frequency

The estimated value is 593 KΩ and the closed-loop input resistance for a voltage follower would be $R_{in.CL}=R_{in,OL}(1+|T|)$ (voltage summing type) where *T* is the loop gain. For the non-inverting unity-gain configuration, *T* is approximately equal to A_{OL}. Thus $R_{in,CL}$ = 9.4 GΩ at DC. 9.85 GΩ was obtained in simulation and from this $R_{in.OL}$ = 621 KΩ was calculated and plotted as shown in Figure 4.8(A).

4.6.2 Output resistance

The output resistance is the resistance looking into the output of the op amp and by referring to Figure 3.6 we can describe this by,

$$R_{out,OL} = \frac{1}{g_{o:Q13} + g_{ds:M10}} \tag{4.9}$$

using values of $g_{o:Q13}$ = 250 nS and $g_{ds:M10}$ = 1.2 μS for a tail current of 20 μA, a $R_{out,OL}$ = 680 KΩ was obtained. The value obtained in simulation for the open-loop output resistance, by using an ideal current source at the output and measuring the voltage at the output node, was 500 KΩ. This value as obtained in simulation is shown in Figure 4.8 (B)

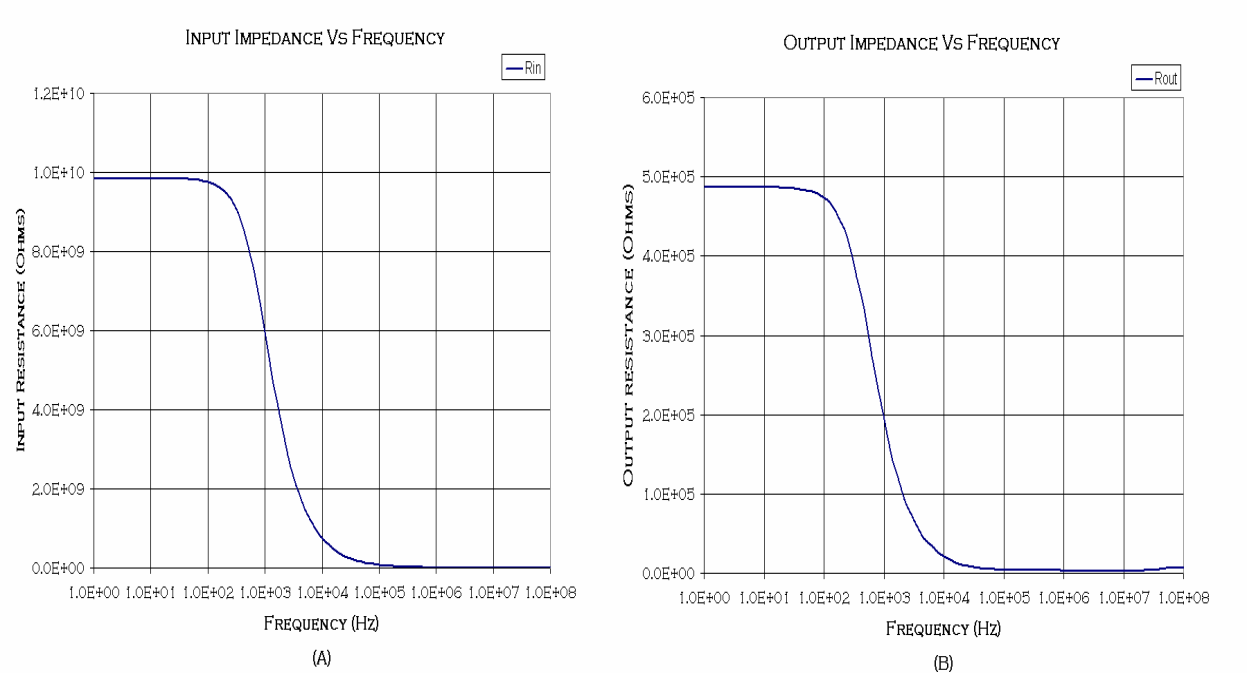


Figure 4.8 Simulated input closed-loop (A) and output open-loop (B) impedances

The closed loop output resistance is given by $R_{out,CL}=R_{out.OL}(1+|T|)$ and this value calculated was 60 Ω. The value observed in simulation was 48 Ω. This op amp is intended to primarily drive on-chip capacitive loads and thus the high output resistance will not limit the applications of the op amp.

4.7 Input Common Mode Range

The limit on the input common-mode voltage level that can be applied to the input terminals of the op amp, such that all the devices remain in the required region of operation, is given by the input common mode range (ICMR) parameter. In the op amp under study, all the input stage PMOS devices are required to be in saturation and all the HBT devices in the forward active region. Based on this criterion, it can be shown that the minimum voltage to keep the HBT devices in forward active, by referring to Figure 3.6, is

$$V_{CM\,(\min)} = V_{BE:Q1} + \left(V_{CE:Q4}\right)_{sat} + V_{SS} \tag{4.10}$$

The resistors at the emitters of Q4 and other current mirrors in op amp's bias circuitry are very small (about 25 Ω) and are used to enhance output impedance. The voltage

drop across them is comparatively negligible. The minimum voltage required for V_{CE} is the saturation voltage to keep the device in forward active region. The value of V_{BE} is the forward active turn-on voltage of HBT devices (about 0.7 V). The maximum voltage that can be applied on the inputs such that the PMOS devices remain in saturation is shown as

$$V_{CM(\max)} = V_{DD} - (|V_{THP}| + V_{SD,sat})_{M4} - \left(V_{CE:Q1}\right)_{sat} + V_{BE:Q1} \tag{4.11}$$

The calculated ICMR range for dual supply was

$$(0.8 - |V_{SS}|) < ICMR < (V_{DD} - 0.6) \tag{4.12}$$

The simulated range for the input common mode voltage with unity-gain feedback was

$$(0.6 - |V_{SS}|) < ICMR_{SIM} < V_{DD} \tag{4.13}$$

This difference in ICMR is because the Q4 tail current device will be able bias the input stage even when it enters the saturation region and thus V_{CE} of Q4 can be somewhat compromised. The values provided by the hand calculations represent a worst case estimate of input common-mode voltage range that can be applied. An optimistic ICMR was predicted in simulations as shown in Figure 4.9. The variation of ICMR with temperature is also provided in Figure 4.9.

4.8 Common Mode Rejection Ratio (CMRR)

The op amp amplifier is designed to amplify the difference in voltage applied to its input terminals and reject the signals common to both. The ability of the circuit to reject the common-mode input voltage is quantified as common-mode rejection ratio and this parameter is very important for the precision of the amplifier. CMRR is defined as the ratio of the differential gain, A_{OL}, to the common mode gain, A_{CM}.

Considering the input stage will give an intuitive understanding of the finite CMRR. The common-mode signal does not see the node at the emitters of Q1 and Q2 shown in Figure 3.6 as an AC ground [11],[25] and when there is an equivalent resistance for the tail current source at that node then a common-mode gain exists. When there is any change in the common-mode signal, there will be a path for it to reach the output of the op amp. The CMRR circuit used for measurement of CMRR and the circuit configurations for other parameters are presented in Chapter 5. The CMRR simulated across frequency is shown in the Figure 4.10.

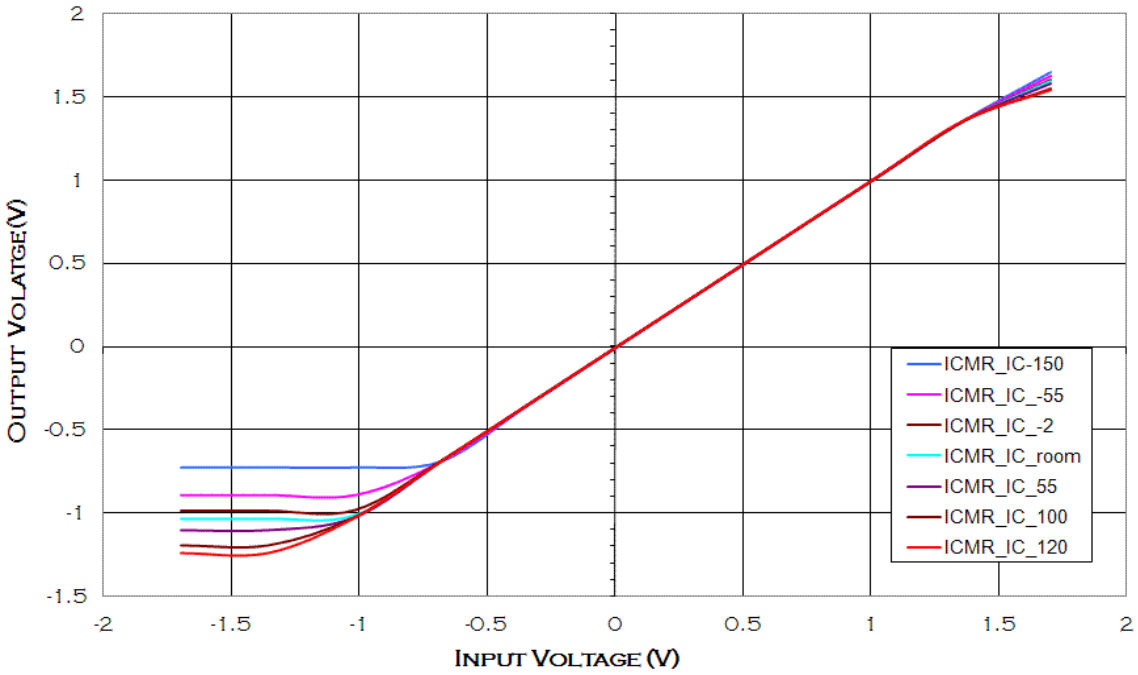


Figure 4.9 Input Common Mode Range

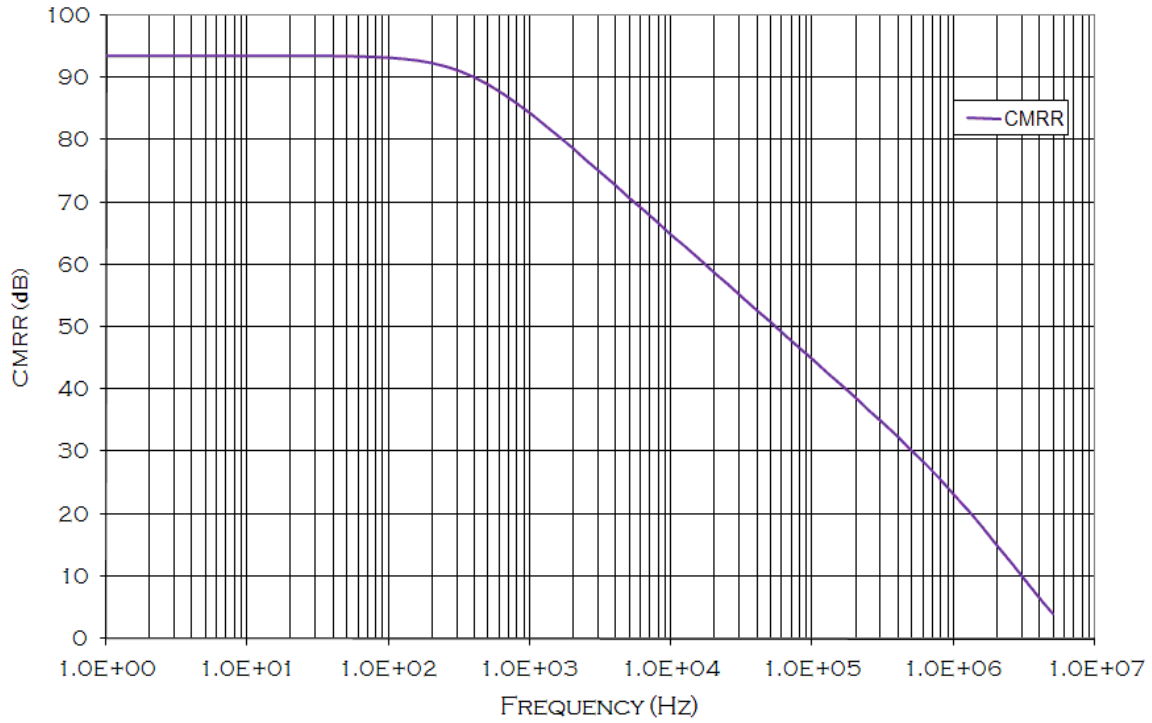


Figure 4.10 CMRR Vs Frequency

4.9 Input Referred Noise Voltage and Current

The noise of the amplifier is dominated by the noise of its input stage since it gets the maximum gain to the output than the rest of the circuit. The input referred noise voltage can be given as

$$e_{ni} = \frac{(e_{n1}A_{v2}) + e_{n2}}{A_{ol}} \tag{4.14}$$

where, e_{ni}, e_{n1}, e_{n2} are the input referred noise of op amp, noise contributed by the input stage and noise contributed by output stage, respectively. A_{v2} and A_{ol} are the gain of the second stage and the entire op amp, respectively. The noise from the current bias circuit is common-mode and therefore negligible in the differential path. By simulation, the input referred voltage noise was obtained as shown in Figure 4.11. This was obtained for a non-inverting unity-gain configuration of the op amp. Since it is an HBT input op amp, the flicker noise should be less than that of a comparable MOSFET input op amp.

The HBT devices, as the input devices, also contribute input referred current noise. A simulation was performed using a non-inverting unity-gain configuration with the positive input node going to ground through a R_S = 1 MΩ resistor. The input referred voltage noise will now be the current noise (i_n) times R_S, along with the thermal noise of the resistor itself, as well as op amp voltage noise (e_n), as given in equation 4.15 [21].

$$e_{ni(total)}\left(\frac{Volts}{\sqrt{Hz}}\right) = [4kTR_S + e_n^2 + (i_n R_S)^2]^{\frac{1}{2}} \tag{4.15}$$

The thermal noise contribution of the resistor may be removed through quadratic subtraction to obtain the input referred current noise. The graph obtained for the input referred current noise is shown in Figure 4.12.

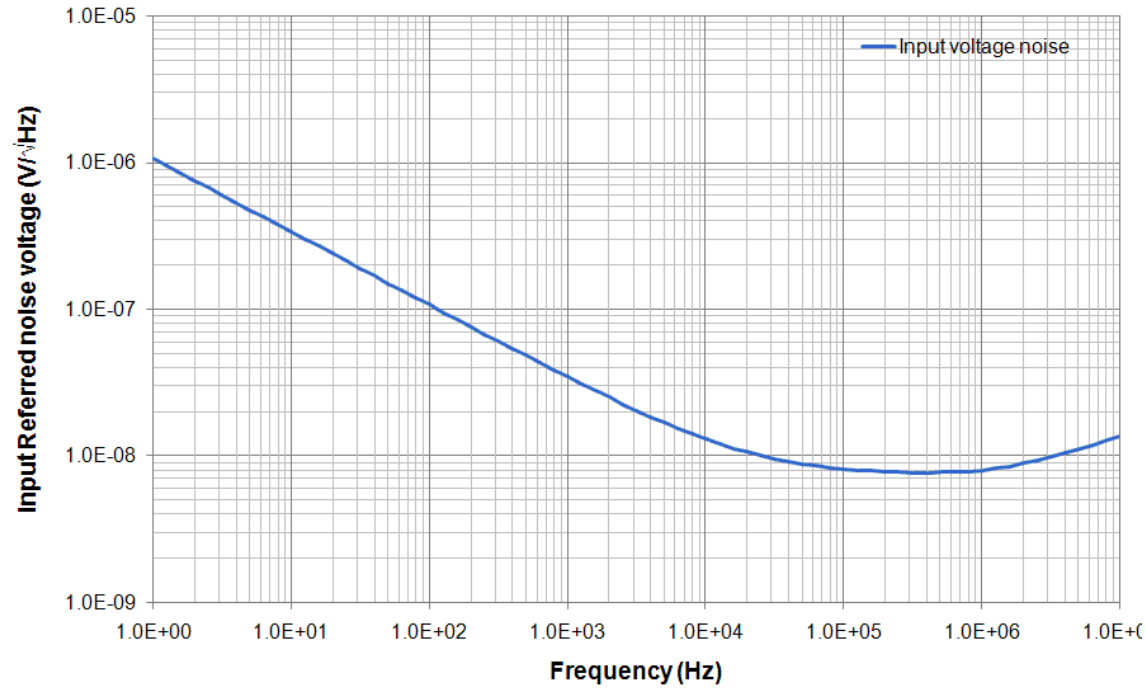


Figure 4.11 Input referred voltage noise

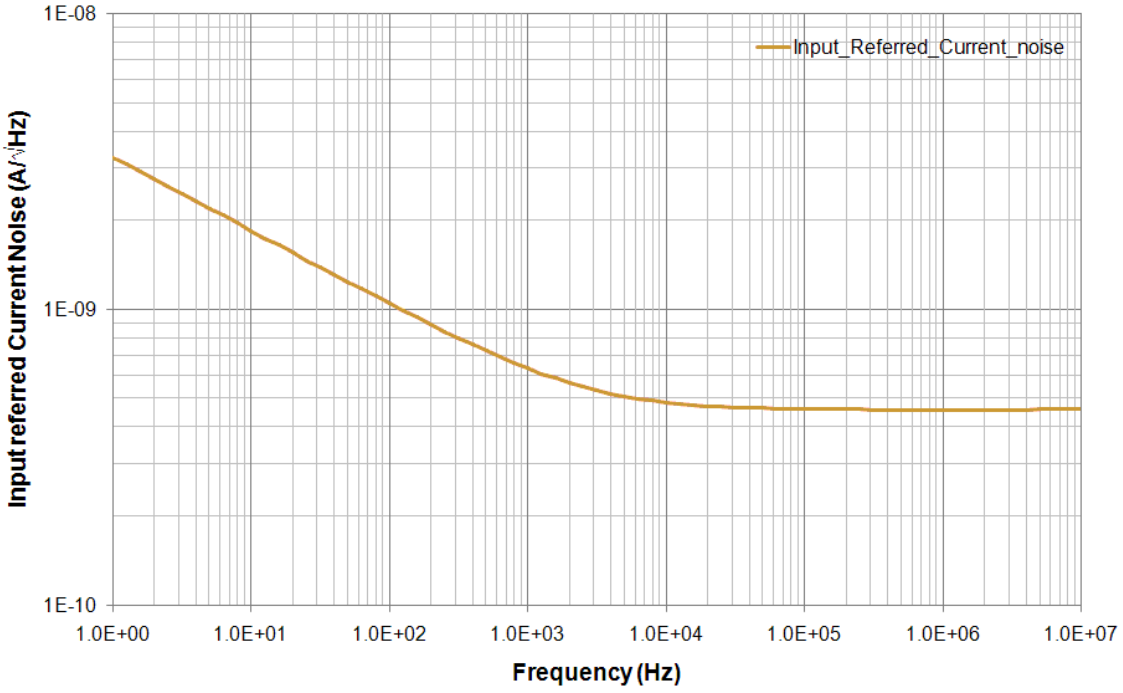


Figure 4.12 Input referred current noise

5 Chapter

Experimental Setup and Test Results

The op amp test chip (*Dium*) bonding after fabrication resided in a 40-pin dual inline package (DIP) and the bonding diagram is shown in Figure 5.1(A). The chip had other circuits with one of them being the constant inversion coefficient (IC) current source circuit. The pin-out for the actual chip after bonding is shown in Figure 5.1(B). This pin-out configuration was used to design the printed circuit board (PCB) required for testing the op amp. To enable more efficient testing, the developed test board supports 4 copies of the *Dium* test chip, each of which contains the SiGe BiCMOS low power op amp.

The PCB was designed using Easily Applicable Graphical Layout Editor (EAGLE) 4.16 software [26] as a 2-layer board. The top layer had all the components and routing and the bottom layer served as a ground plane. The layout of the PCB that was designed for testing the op amp is shown in Figure 5.2.

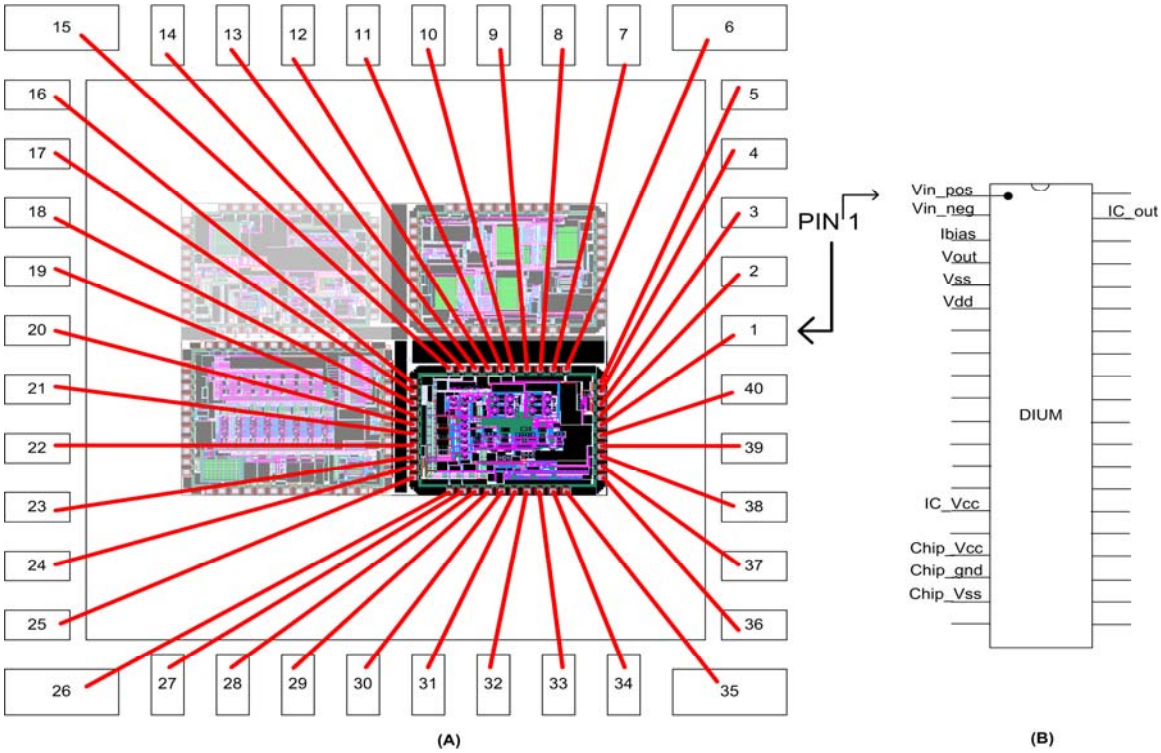


Figure 5.1 Bonding diagram (A) and pin-out (B) for the *Dium* chip

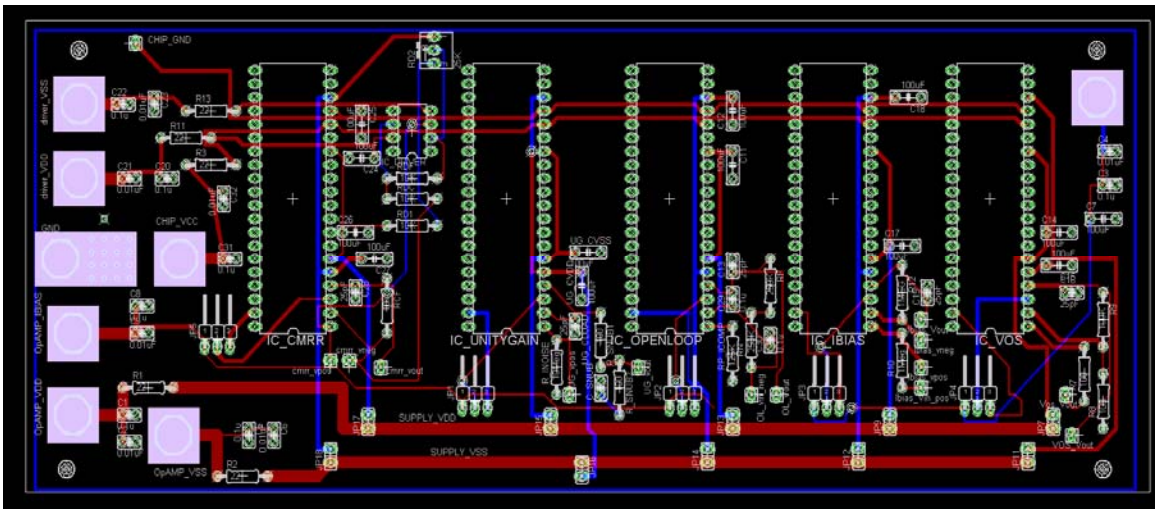


Figure 5.2 PCB layout for testing op amp

For the *Dium* test board, wide traces were run for V_{DD} and V_{SS} to provide low resistance power supply rails. Filtering of power supply noise was done by using 0.1 µF and 0.01 µF ceramic capacitors, as well as 100 µF electrolytic capacitors. A 22-Ω resistor separated the electrolytic and ceramic capacitors to form a filter network on each power supply rail.

The red tracks in Figure 5.2 are the tracks on the top layer and the blue tracks are the few tracks that are cut through the polygon of the bottom layer on which a large polygon of ground is present. 2-pin jumpers were used for controlling the power flow into each circuit and 3-pin jumpers to choose the current IBIAS for the op amp on each duplicate test chip. The chip as shown in Figure 5.1 has the constant IC current source that was used as one option for biasing of op amp, with the Keithley 2400 source meter being the other option.

The results provided for various parameters are for constant IC bias and comparisons of the parameters for 3 types of current biasing: proportional-to-absolute-temperature (IPTAT), constant IC, and constant current. These comparisons are provided in the last section in this chapter.

5.1 Input Common Mode Range (ICMR)

The input common-mode range was measured using the unity-gain follower configuration as shown in the Figure 5.3. The input Vin was a DC ramp signal and it

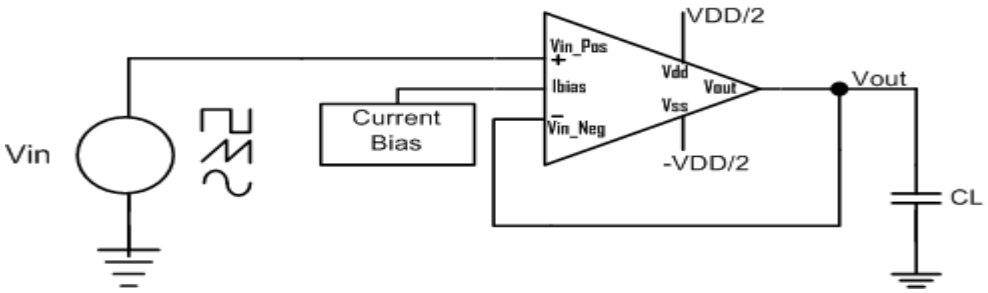


Figure 5.3 Voltage follower (unity-gain) Circuit

was swept from −1.7 to +1.7 V using the Keithley 2400 source meter. The output was measured using the HP 34401A multi-meter and it was plotted using a Labview program. As expected, it was observed that the output follows the input as long as the circuit is in the input common mode range and deviates when the devices go out of the quiescent region of operation. The calculated and simulated values for ICMR were provided in Chapter 4 and the measured ICMR range is provided in Figure 5.4. The measured results agree well with the simulated and calculated results.

5.2 Open Loop Gain and Unity Gain Bandwidth

The circuit used for measuring the open-loop gain is as shown in Figure 5.5. Since the open-loop gain for the op amp is over 60 dB, measuring A_{OL} in the open-loop configuration will not give accurate results. Thus, the error gain method was used in the inverting unity-gain configuration to measure the open-loop gain based on equation 5.1.

$$A_{ol} = \frac{V_{out}}{V_e} \tag{5.1}$$

Network analyzer HP3589 was used to source 1 $V_{P\text{-}P}$ as Vin and error voltage V_e was given as the input to the analyzer for measurement in dBV. A Labview program was used to control the network analyzer source and measure the voltages. Equation 5.2 was used for the calculation of A_{OL} across various frequency ranges. The values obtained over temperature across these frequency ranges are shown in Figure 5.5.

$$A_{OL} = 20 \cdot \log\left[\frac{V_{out}}{10^{dBV_e/20}}\right] \tag{5.2}$$

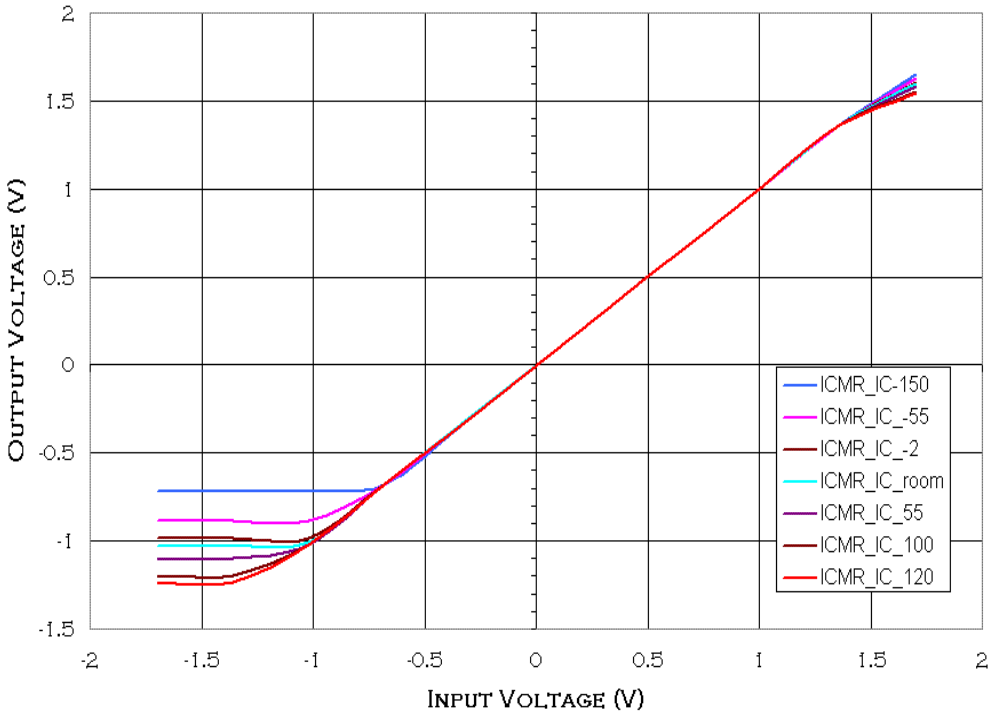


Figure 5.4 Measured input common mode range over temperature range

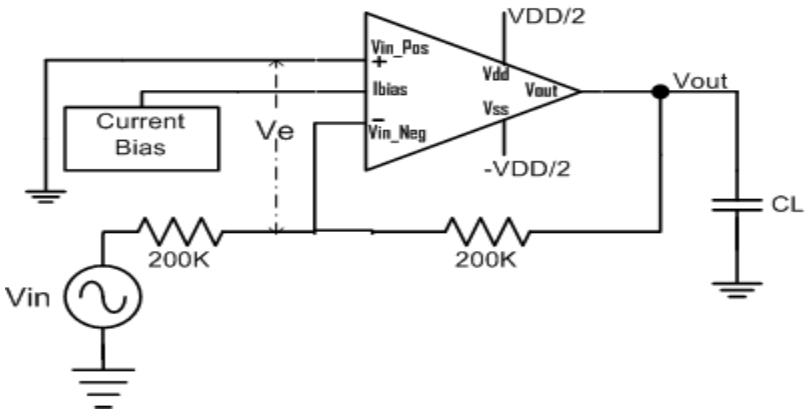


Figure 5.5 Measurement circuit for open-loop gain (error gain)

The measured results showed an increase in A_{OL} with decrease in temperature as shown in Figure 5.6, as expected and observed in simulations. The unity-gain bandwidth for the circuit was observed to be around 7 MHz for various temperatures based on the extrapolated values.

5.3 Slew Rate (SR)

Slew rate was measured using the voltage follower circuit shown in Figure 5.3. Vin was given as a 2 V_{P-P} square wave with a 100 KHz frequency using the HP 33250A function generator and the output was measured using the Agilent 54622D oscilloscope. The slew rate observed is as shown in Figure 5.7.

5.4 Input Bias and Offset Currents

The circuits used to measure the input bias currents are shown in Figure 5.8. The output voltage from each circuit will be the sum of offset voltage and voltage across the resistor due to input bias current as described in equation 5.3.

$$V_{out} = V_{os} + I_{bias} R \tag{5.3}$$

The values of offset voltage and input bias currents can be in the μV and nA range, respectively. Since the resistor value chosen is 1 MΩ, the output voltage is dominated by input bias current. Based on equation 5.3, the value of the input bias currents were calculated from measured data across temperature as shown in Figure 5.9. Power supply HP E3631A was used to provide V_{DD} and V_{SS} and the multi-meter HP 34401A was used to measure the output DC voltage.

The value of input bias current is the average of the bias current flowing into the positive and negative input terminals as shown in the equation 5.4 and the input offset current is the difference between the two input bias currents as shown in equation 5.5. This is plotted in Figure 5.9. The measured $|I_{OS}|$ remains below 10 nA across temperature.

$$I_B = \frac{I_B^+ + I_B^-}{2} \tag{5.4}$$

$$I_{OS} = \pm | I_B^+ - I_B^- | \tag{5.5}$$

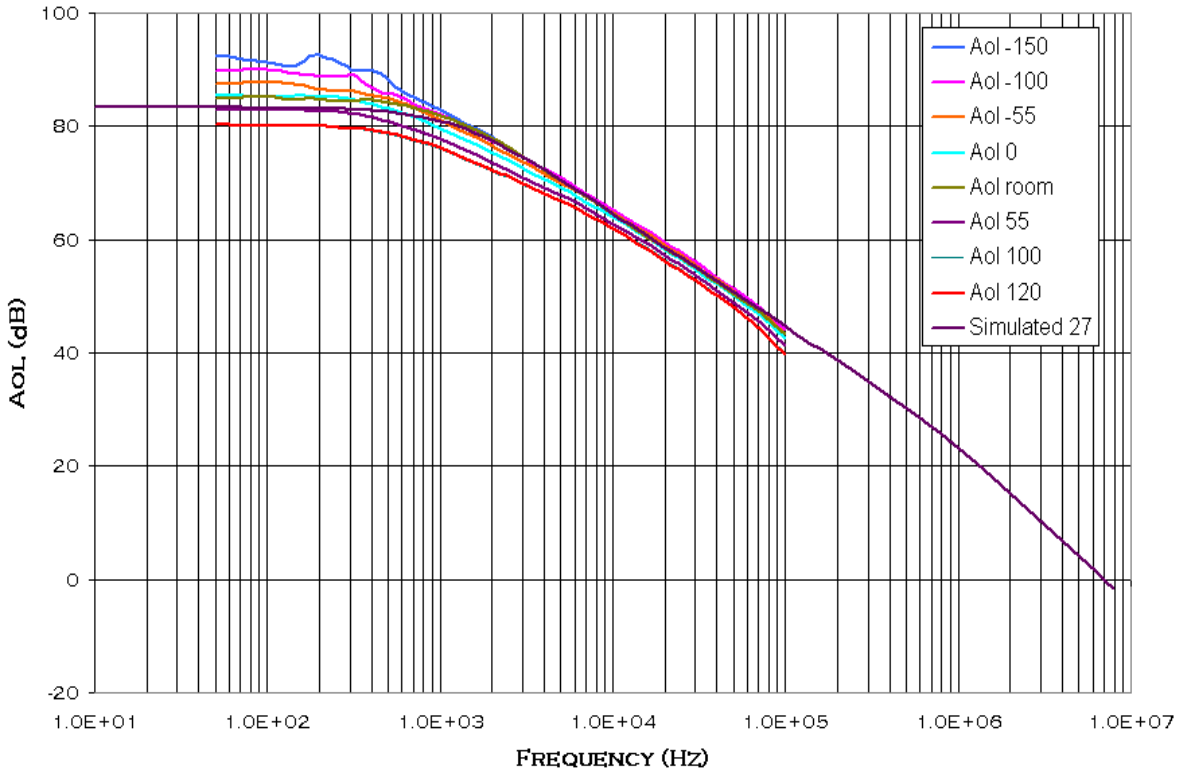


Figure 5.6 Measured open-loop gain vs. frequency over temperature

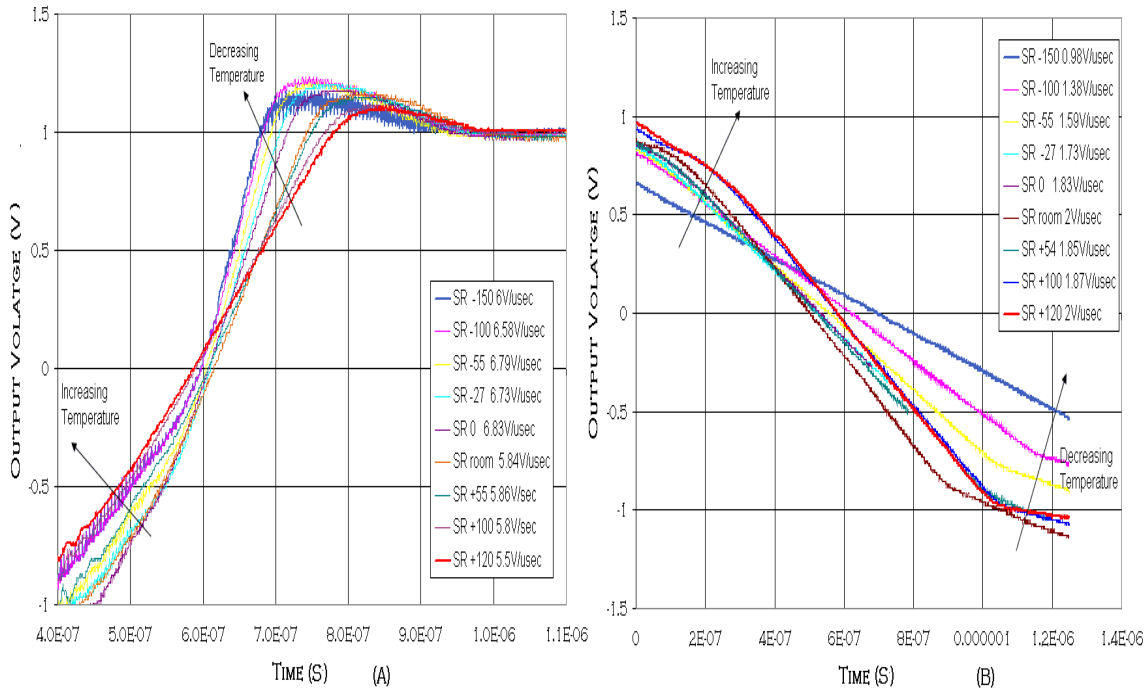


Figure 5.7 Measured large-signal positive-going output (A) for SR+ and negative-going output (B) for SR− over temperature

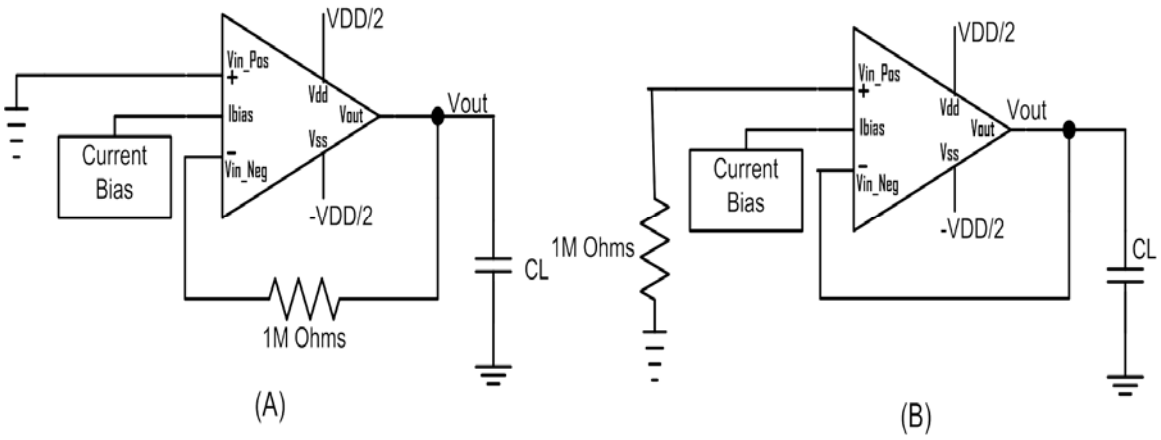


Figure 5.8 Input bias current measurement: I_{BIAS}^{-} (A) and I_{BIAS}^{+} (B) circuit configurations

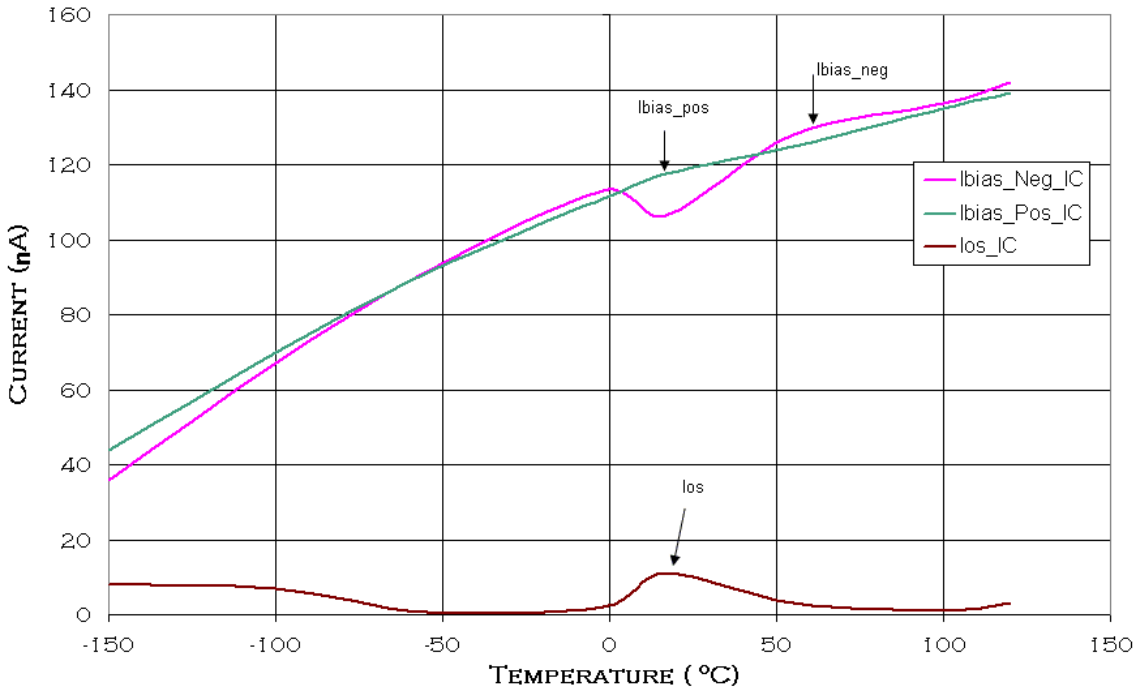


Figure 5.9 Measured input bias and offset currents across temperature

5.5 Power Supply Rejection Ratio

The power supply rejection ratio was measured using the voltage follower circuit shown in Figure 5.10. The supply was sweep across a small range from 3 V to 3.6 V in 0.02 V steps. The software program for Labview that was developed in ICASL [27] was used for this measurement. The software was used for sweeping the supply voltage and measures the output voltage using a multimeter. The software then calculates the PSRR using equation 5.6. The measured DC PSRR is plotted for different temperatures in Figure 5.11.

$$PSRR = \frac{dV_{DD}}{dV_{OUT}} \tag{5.6}$$

5.6 Input Offset Voltage

The input offset voltage is measured using the unity-gain follower circuit that was used for PSRR measurement as shown in Figure 5.10. The difference in this measurement is that V_{DD} is kept constant and the output is measured. The output voltage should be near zero since the input is at zero when a complimentary dual supply voltage is used. Any deviation of the output from zero is a measure of the offset voltage. Since the circuit was in unity-gain feedback and no resistors were used in the circuit, the input bias currents and offset current will not affect the measurement values. The plot obtained for measured V_{OS} across temperature is provided in Figure 5.12. For these measurements an (on-chip) constant IC current source circuit was used to bias the op amp.

5.7 Comparison of Various Bias Techniques

The bias current required by the op amp can be provided using various bias techniques such as current proportional-to-absolute temperature (I_{PTAT}), current with constant inversion coefficient over temperature (constant IC) [28] and current constant over temperature. Each bias current technique can affect the performance parameters of the op amp across temperature. The purpose of this section is to analyze the effect of I_{PTAT}, constant IC and constant current biasing on the characteristics of the op amp.

Traditionally I_{PTAT} current is used for BJT circuits to maintain constant transconductance constant over temperature, as seen from equation 5.7.

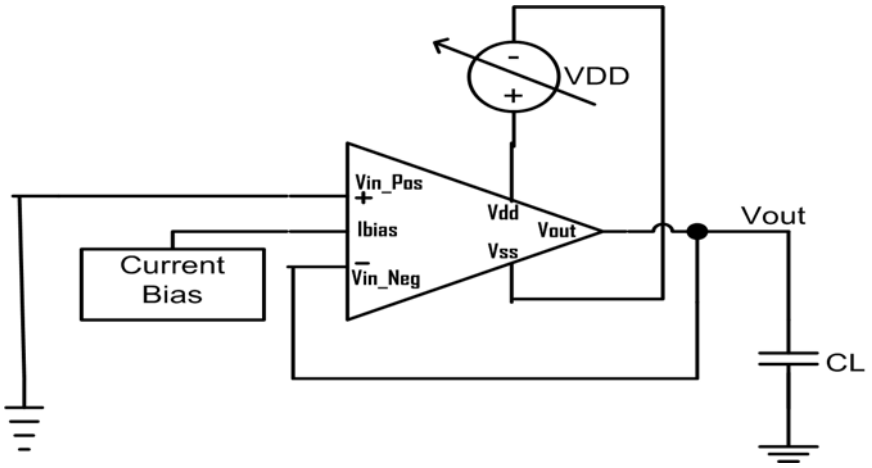


Figure 5.10 PSRR measurement circuit

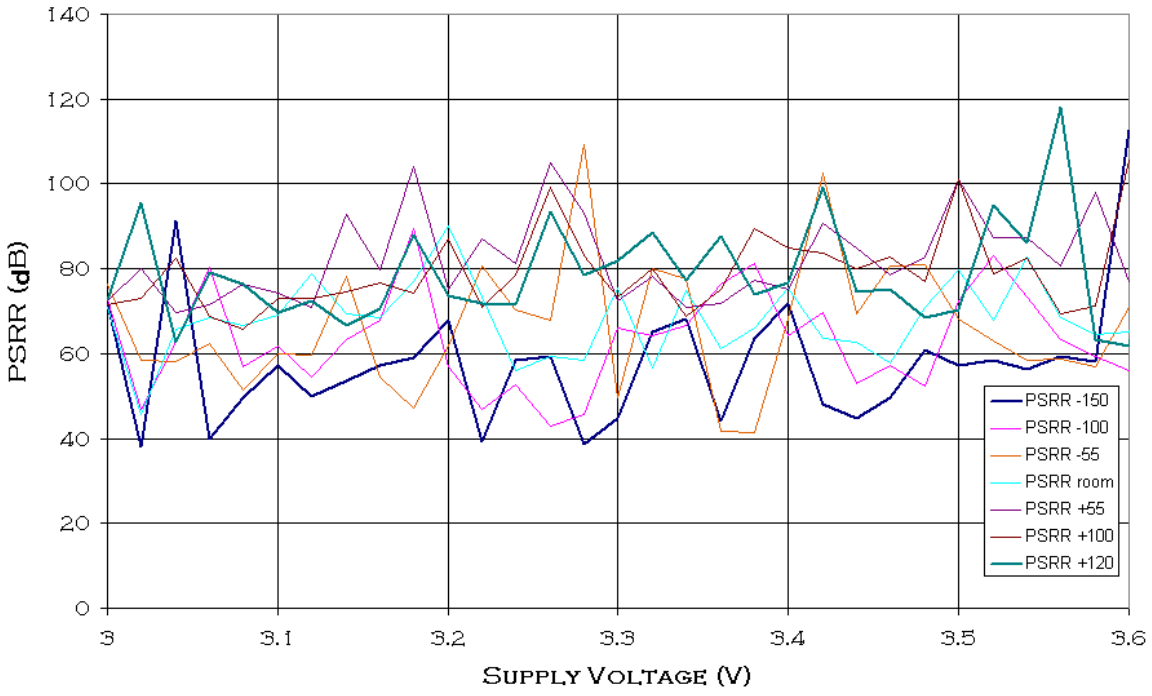


Figure 5.11 Measured DC power supply rejection ratio over temperature

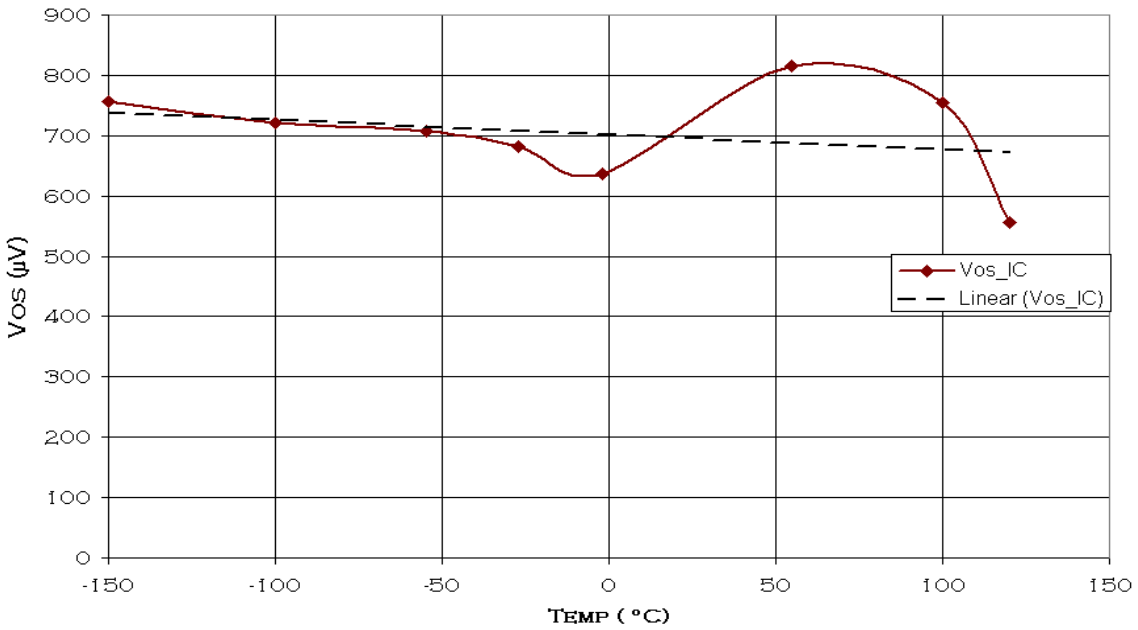


Figure 5.12 Measured input offset voltage variation across temperature

$$g_m = \frac{I_C}{V_t} \tag{5.7}$$

where I_C is the collector current and $V_t = kT/q$ is the thermal voltage. Since V_t is proportional to absolute temperature and the collector current is also proportional to absolute temperature, then constant transconductance is maintained. Therefore op amp bandwidth should be constant over temperature.

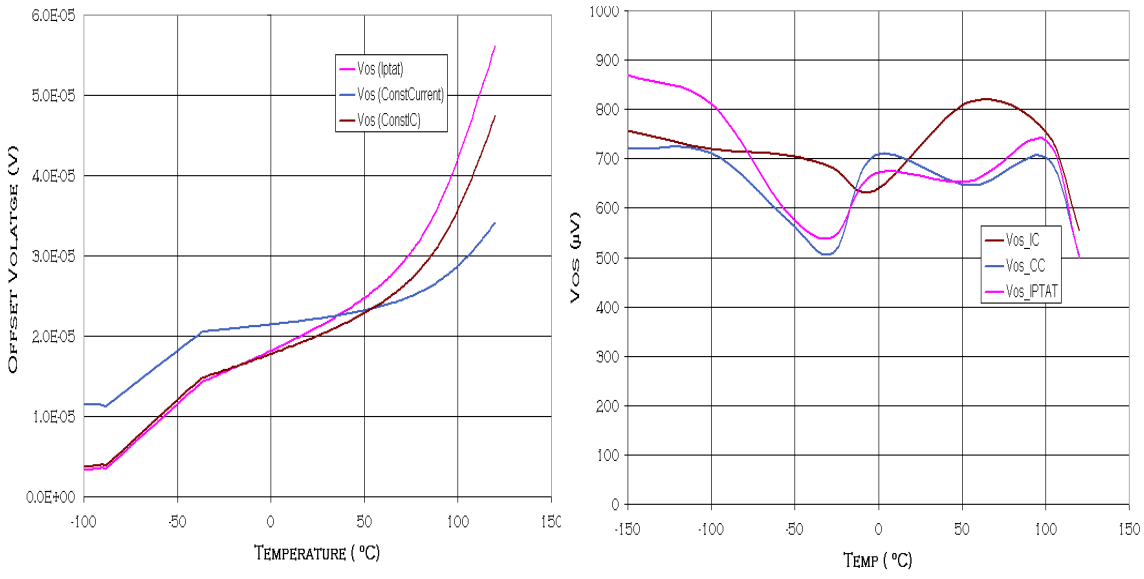
In case of MOSFETS, a bias technique that makes the g_m/I_D ratio constant over temperature is preferred for wide temperature operation [28]. The equation for the transconductance parameter over temperature is given as

$$g_m = 2\frac{I_d}{V_{eff}} \tag{5.8}$$

where I_d is the drain current and $V_{eff} = V_{GS} - V_{THN}$ is the effective gate-source voltage. When g_m/I_d is made constant over temperature, we find that effective gate-source voltage becomes constant over temperature. This implies constant inversion level (quantified by IC) over temperature, thus enabling CMOS analog circuit performance to be optimized over temperature since MOSFET characteristics are tied to inversion level.

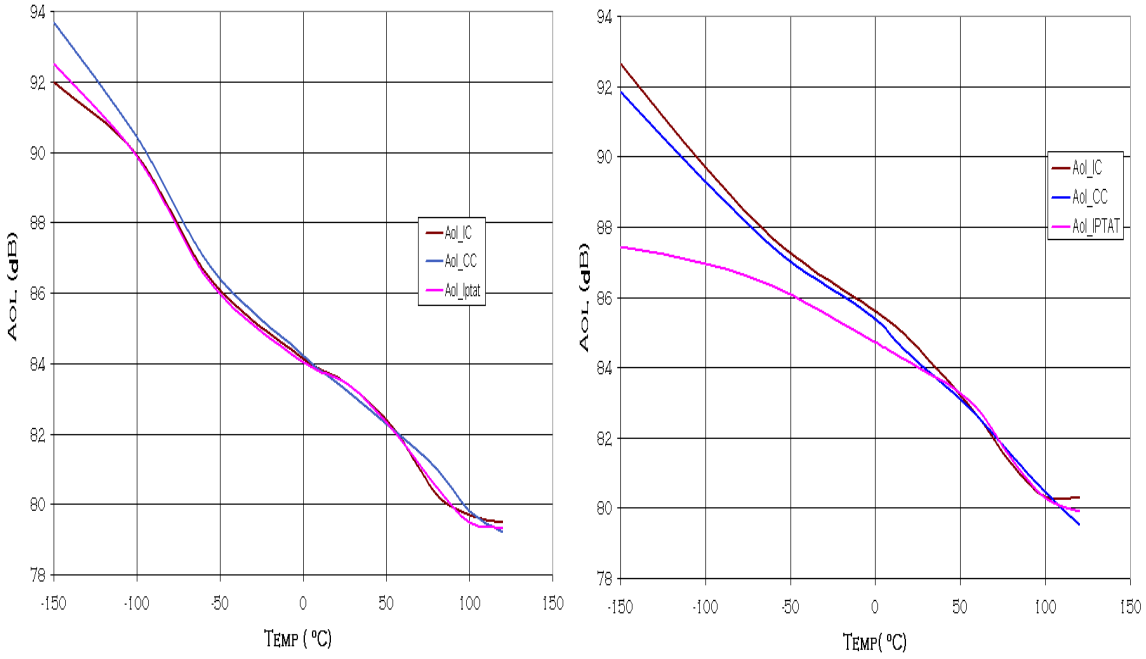
Since the SiGe low power BiCMOS amplifier has a BJT-like input pair (HBT) and PMOS load, examination of which current bias technique might be more appropriate for the op amp is required. In simulation the drift in the input systematic offset voltage was observed to be minimal for the constant current bias. This difference in the drift was not verified by experiment because of the dominance of random offset on the input offset voltage. The simulated and actual experimental graphs are provided in Figure 5.13. The comparisons of offset voltages in simulation and on test bench only showed that either the constant current or constant IC bias will cause the op amp to have a lower offset voltage drift than the I_{PTAT} current bias technique. Other parameters were compared to help find a clear preference of current bias.

The open-loop gain at a fixed frequency of 50 Hz was measured using the three bias techniques. Simulations did not predict significant variation in A_{OL} over temperature using the three different biasing techniques. The same was observed on the test bench, though there is a small change in the gain using the I_{PTAT} bias technique. The constant current and constant IC bias techniques provide almost the same measured open-loop gain across temperature. These results are shown in Figure 5.14.



(A) (B)

Figure 5.13 Simulated (A) and measured (B) offset voltage variation across temperature for different current bias techniques



(A) (B)

Figure 5.14 Simulated (A) and measured (B) open-loop gain at 50 Hz across temperature for different current bias techniques

The comparisons of measured slew rate across temperature provided similar results. The bias current techniques across temperature yielded similar trends observed in the simulated input offset voltage, i.e. there was the least drift in the input bias currents when using the constant current biasing technique. This was observed both in the simulation and experimental results, as shown in the Figure 5.15. Figures 5.15(A) 5.15(B) show the simulated and experimental variation, respectively, of positive I_{BIAS} across temperature. The negative I_{BIAS} simulation and experimental results are shown in 5.15(C) and 5.15(D), respectively.

In summary, there was no major benefit in using one current bias technique over the others for the SiGe BiCMOS low power op amp. Constant current bias yields lower input bias current variation over temperature, however, and may be considered a better choice over the other two techniques for the parameters tested.

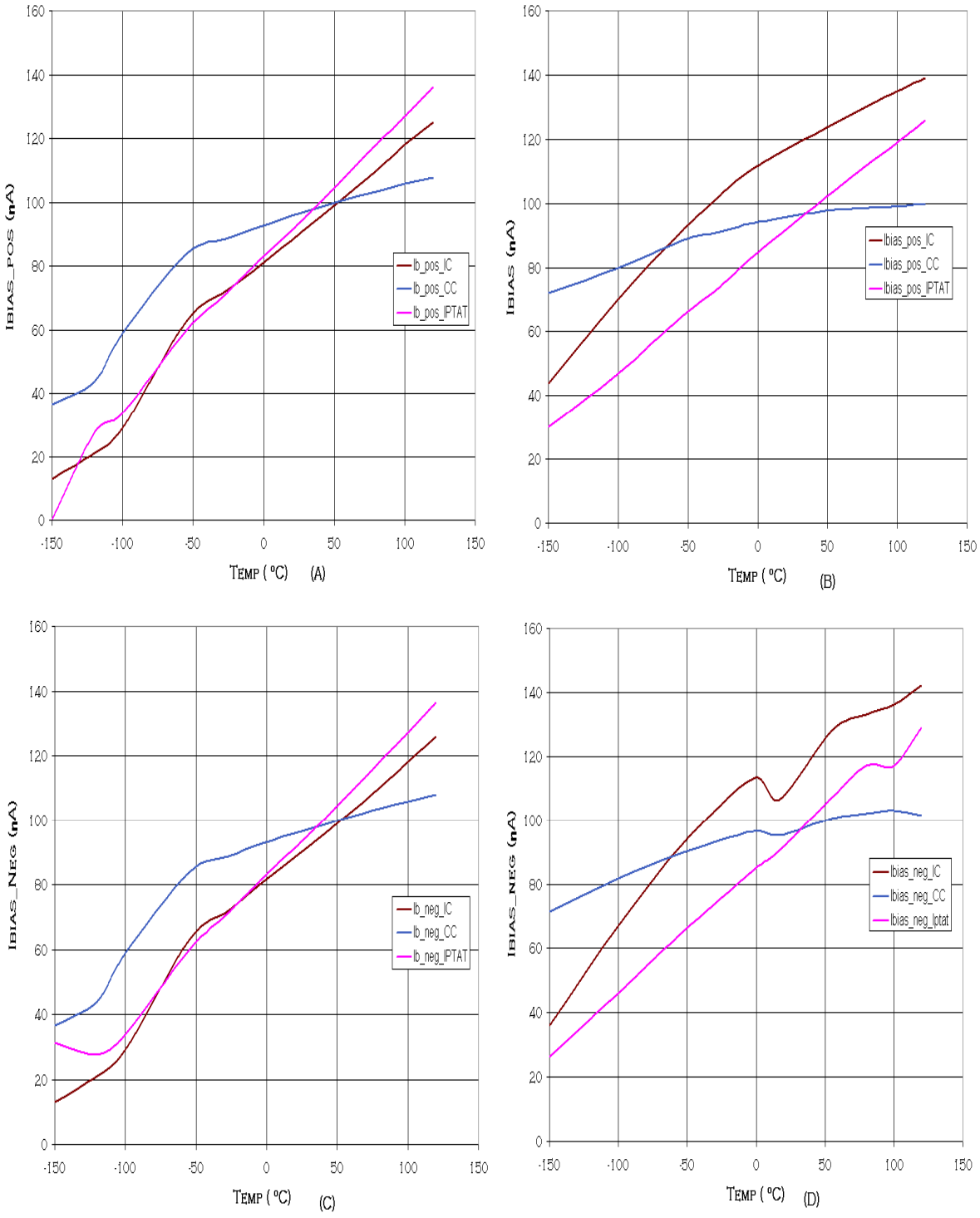


Figure 5.15 Simulated and measured op amp input bias current variation across temperature for different current bias techniques

6 Chapter
Conclusions and Future Work

The analysis and characterization of the SiGe BiCMOS low power op amp has been described in this thesis. This op amp was tested over wide temperature and was found to meet the required specifications. The op amp provides a rail-to-rail output voltage swing, high open-loop gain, low power and low offset voltage as its key features.

The SiGe BiCMOS low power op amp's operation under different bias current techniques (PTAT current, constant current and constant inversion coefficient current) across temperature has been studied. The constant current bias technique proved to be an attractive choice since the op amp then provides nearly constant input bias current across temperature, therefore minimizing this source of offset in circuit applications using the op amp.

Comparison of the BiCMOS op amp with a CMOS op amp counterpart [22] for various required parameters has been done and summarized as shown in Table 6.1. The BiCMOS design consumes lower power with higher unity-gain bandwidth (UGBW).

Table 6.1 Comparison of the results from BiCMOS and CMOS op amp

Parameter (Room Temp)	**Requirement**	**BiCMOS Op amp**	**CMOS Op amp [from 22]**	**Units**
Power consumption	< 1	0.5*	≈1.3	mW
Supply current	< 1	0.16*	0.4*	mA
Open Loop Gain	> 60	84	89	dB
UGBW	> 2	5.5	4.5	MHz
Slew rate	> 2	SR^+ = 6, SR^-=3.3	SR^+ = 8, SR^- = 7	V/µs
Input offset voltage	< 2	0.8	1.6	mV
Input bias current	< 200	100	Negligible	nA
PSRR	> 60	68	65	dB

* The power consumption and supply currents are compared based on simulation. The actual measurement showed less than 1 mW power consumption and less than 1 mA current from the supply.

The future work for this op amp is to integrate the BiCMOS op amp, the hardened version of the BiCMOS op amp (including HBTs that are radiation hardened by design (RHBD) to suppress single-event effects), and the three current bias techniques provided on a single chip. Incorporating RHBD into the BiCMOS op amp design will further broaden its application to extreme environments. For the present op amp testing, only the constant IC circuit was present on the same chip while the other bias techniques (I_{PTAT} and constant current) were not. Testing was done by providing the constant current and I_{PTAT} currents from a Keithley sourcemeter configured as current source. Having a single chip including the op amp and complete biasing options will facilitate easier and more accurate temperature testing. Having all the circuits integrated into the same chip will facilitate radiation testing as well.

The integration of all these circuits has been done and submitted for fabrication in September 2007 and testing will be the next step after chip fabrication is complete. The layout of these circuits along with the pad frame is shown in Figure 6.1. To facilitate the testing of both the hardened and non-hardened version at the same time, 2 leads have been brought out for each type of current bias and it is only a matter of connecting different pins to utilize different current biasing techniques.

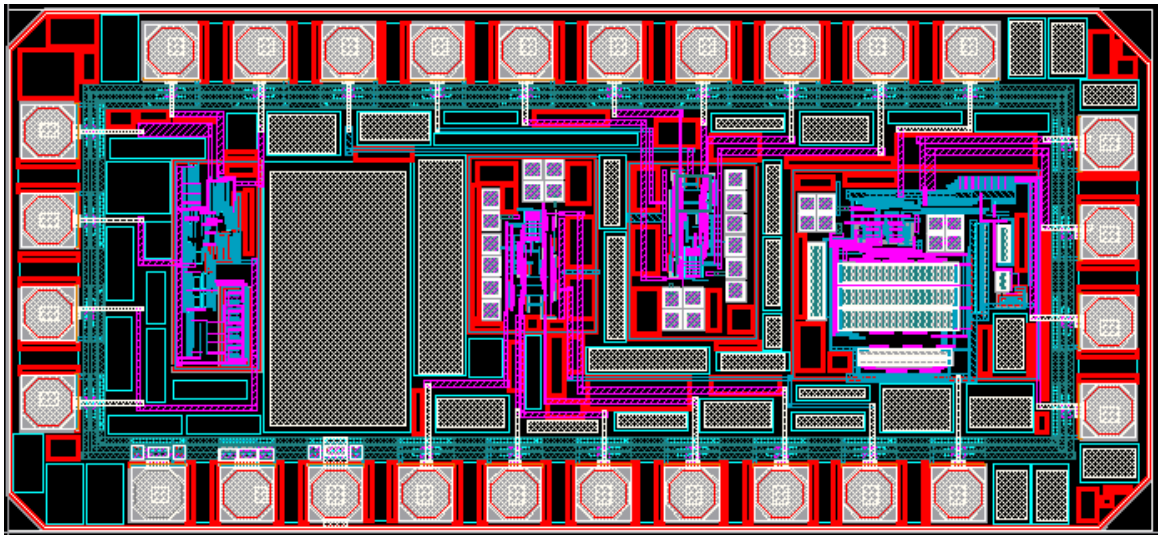


Figure 6.1 Future work test chip includes the original SiGe BiCMOS low power op amp, as well as a radiation-hardened-by-design version of the op amp, and current bias circuits all within the same pad frame

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APPENDIX

A.1 Constant Inversion coefficient current source circuit

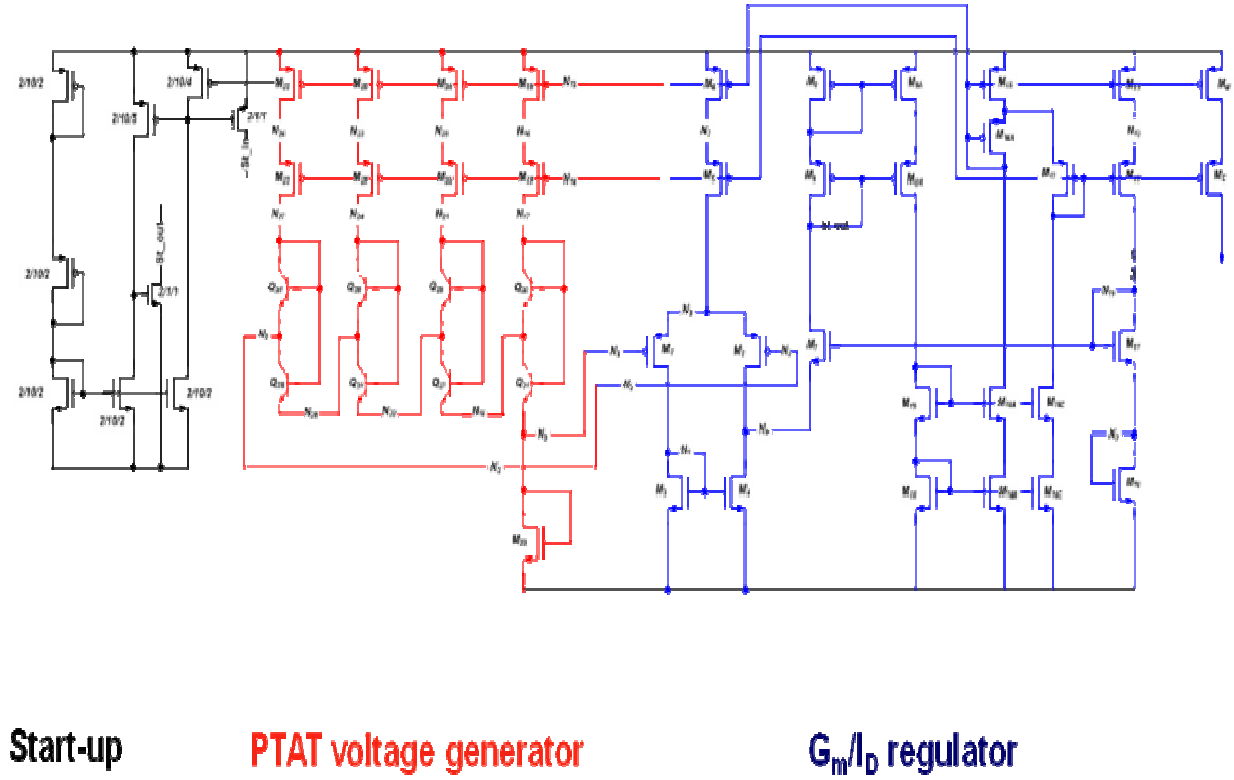

Figure A.1 Schematic of current inversion co-efficient current bias circuit

A.2 Constant current source

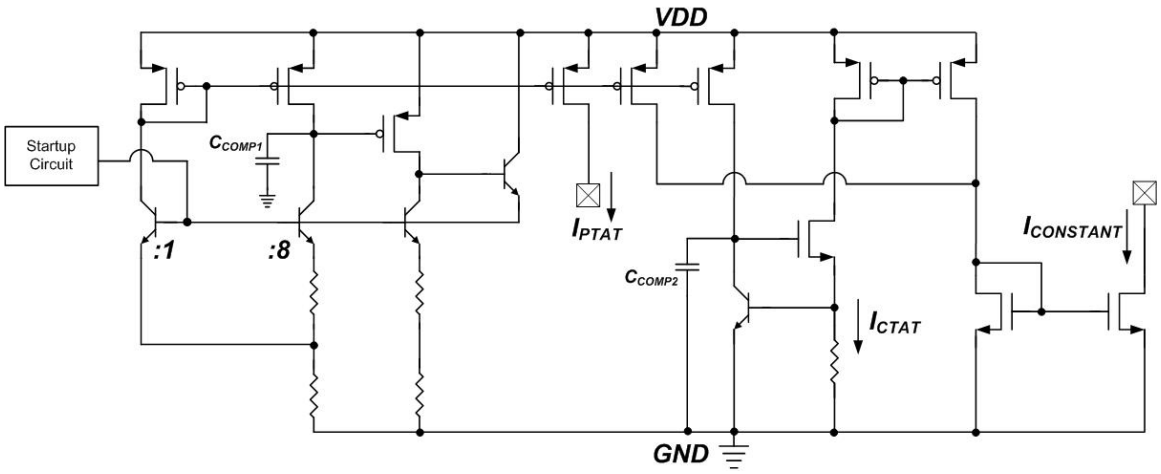

Figure A.2 Simplified schematic of constant current and I_{PTAT} current source technique

VITA

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